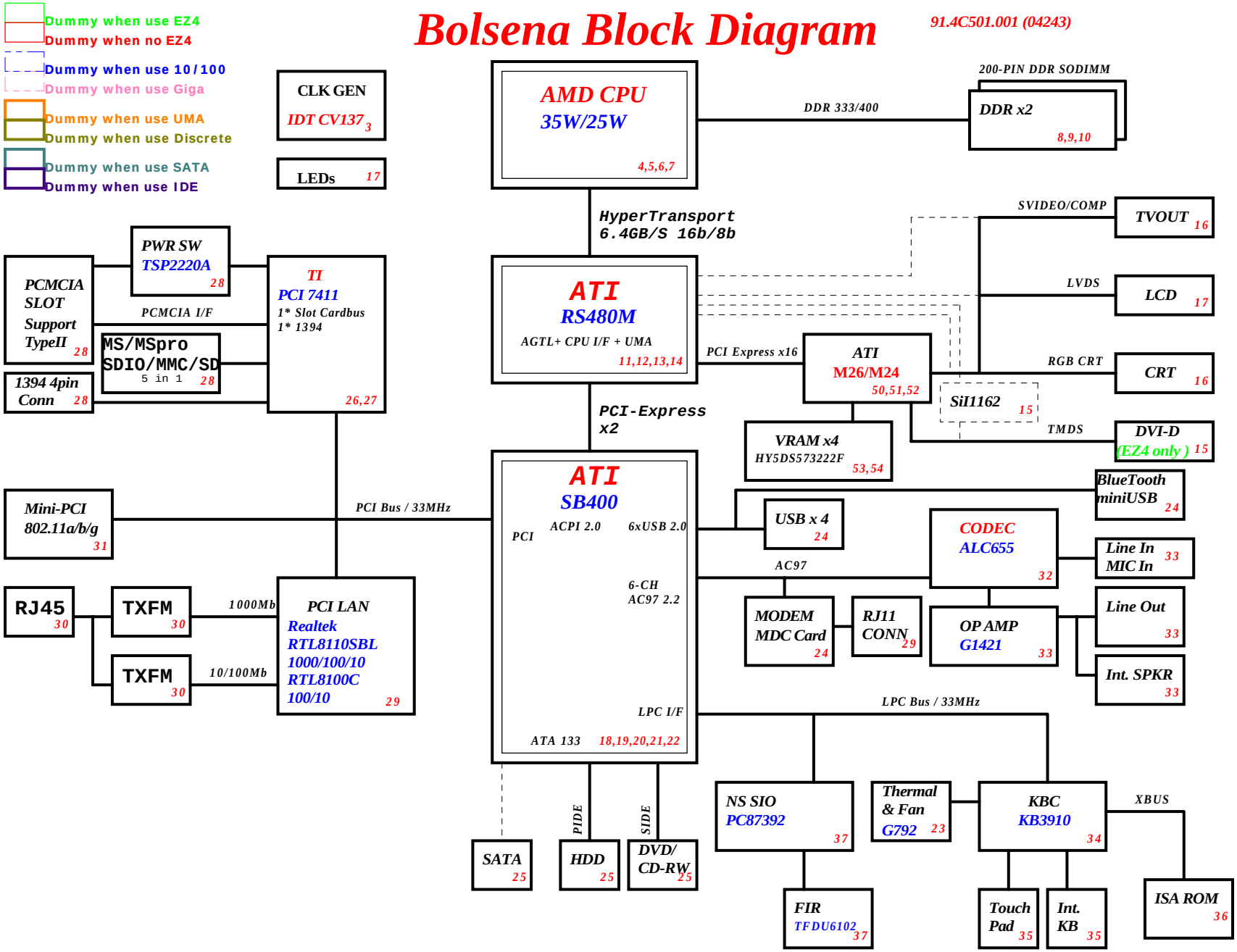
Bolsena Block Diagram

91.4C501.001 (04243)



PCB Layer Stackup
L1: Signal 1
L2: GND
L3: Signal 2
L4: Signal 3
L5: VCC
L6: Signal 4

?modify power block

Battery Charger 48	
INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

SYSTEM DC/DC 44	
INPUT	OUTPUT
DCBATOUT	5V_S5, 3D3V_S5

SYSTEM DC/DC 45,46	
INPUT	OUTPUT
DCBATOUT	2D5V_S3 1D8V_S5 1D2V_S0

CPU V_CORE 42,43	
INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM POWER 47	
INPUT	OUTPUT
2D5V_S3 DCBATOUT	1D25V_S3 5V_AUX_S5

Port Replicator 4 (124 PIN)

AC IN | RJ45-11 | SEARIAL PORT | CRT | PRINTER | PS2 | MIC | LINE IN | LINE OUT | TV OUT | DVI | PCIeX2 | SMBUS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM

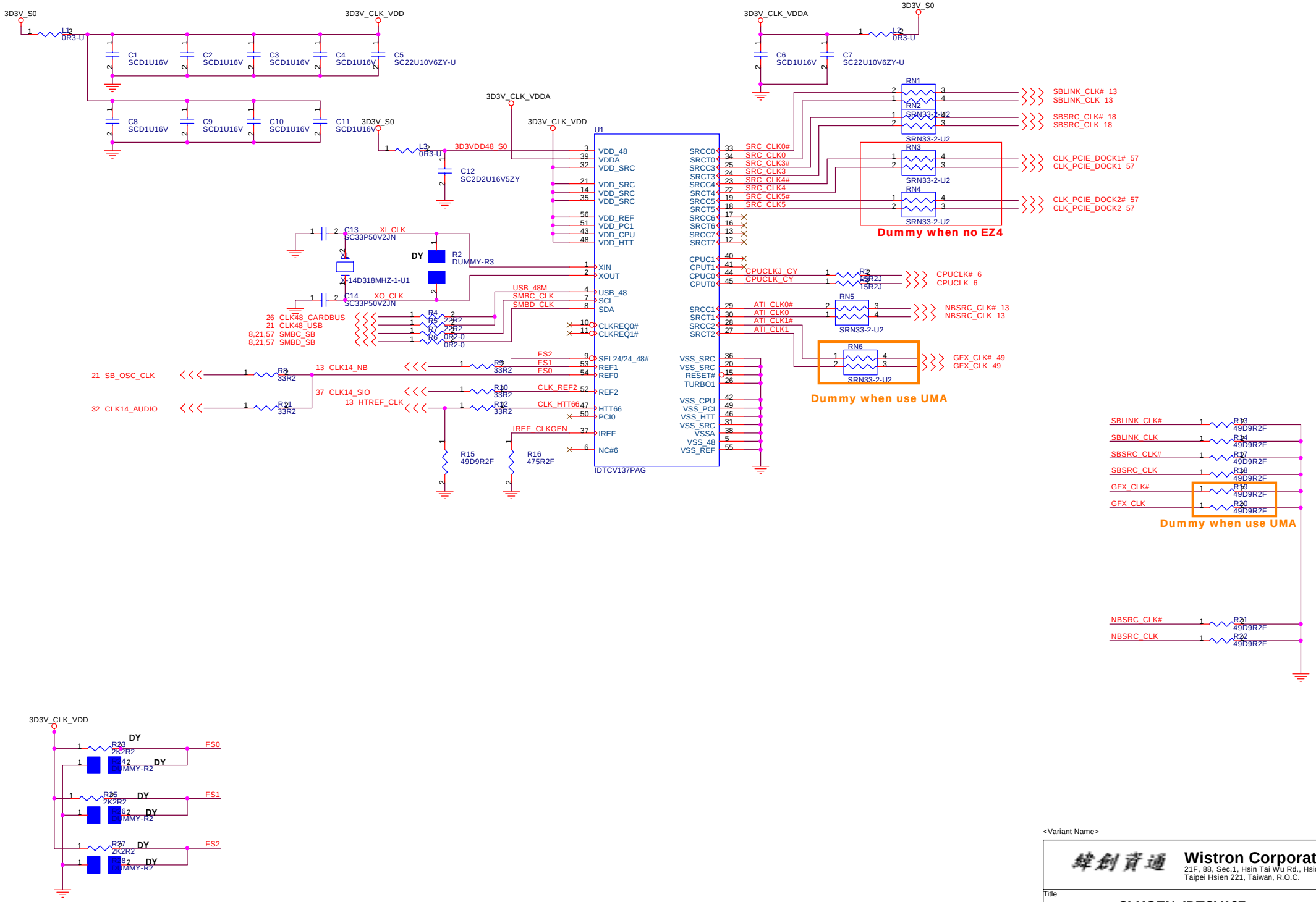
Size: A3 | Document Number: Bolsena | Rev: SA

Date: Tuesday, December 28, 2004 | Sheet 1 of 58

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CHANGE HISTORY	
Size A3	Document Number Bolsena	Rev SA
Date: Tuesday, December 28, 2004	Sheet 2 of 58	



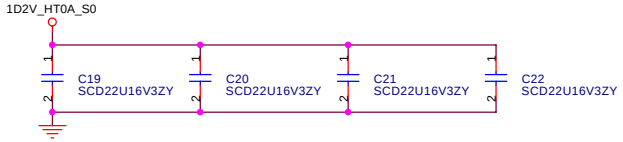
<Variant Name>

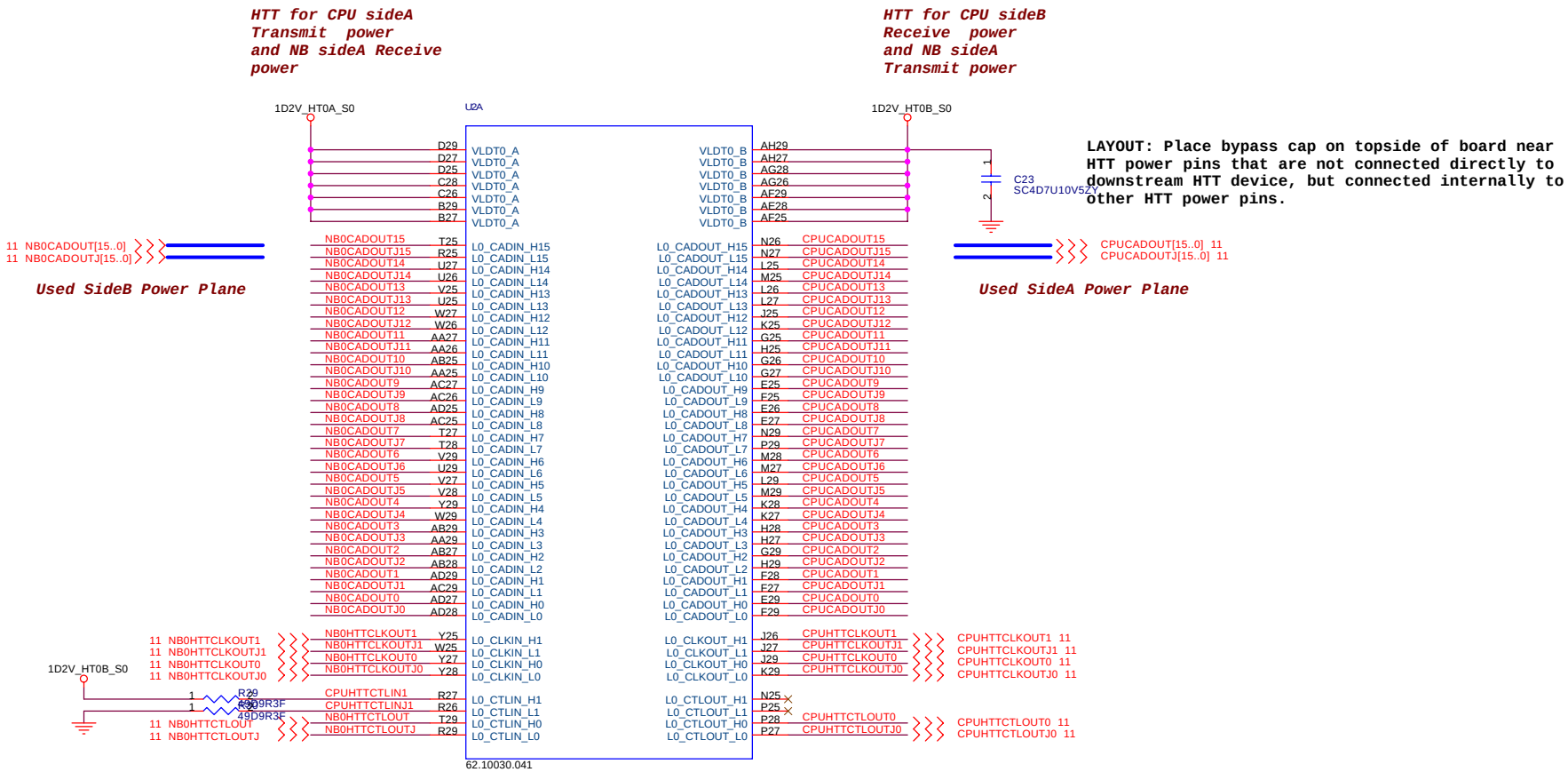
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CLKGEN_IDTCV137**

Size: A3 | Document Number: **Bolsena** | Rev: SA

Date: Tuesday, December 28, 2004 | Sheet 3 of 58





By ME requset U11 P/N:
Main 62.10030.041
Second 62.10053.191
Third 62.10053.201

<Variant Name>

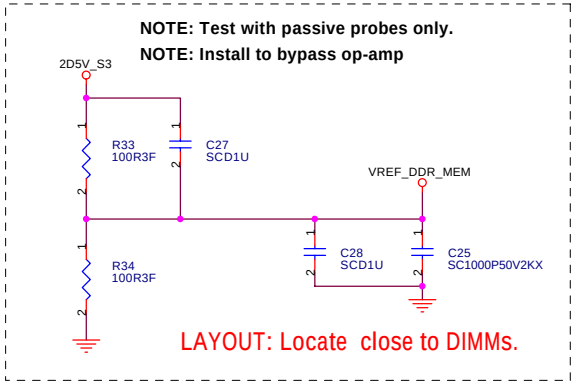
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(1/4)_HyperTransport I/F

Size: A3 | Document Number: Bolsena | Rev: SA

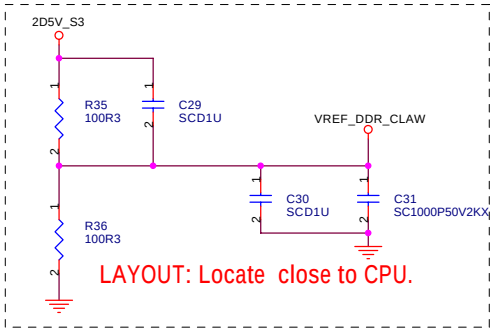
Date: Tuesday, December 28, 2004 | Sheet 4 of 58

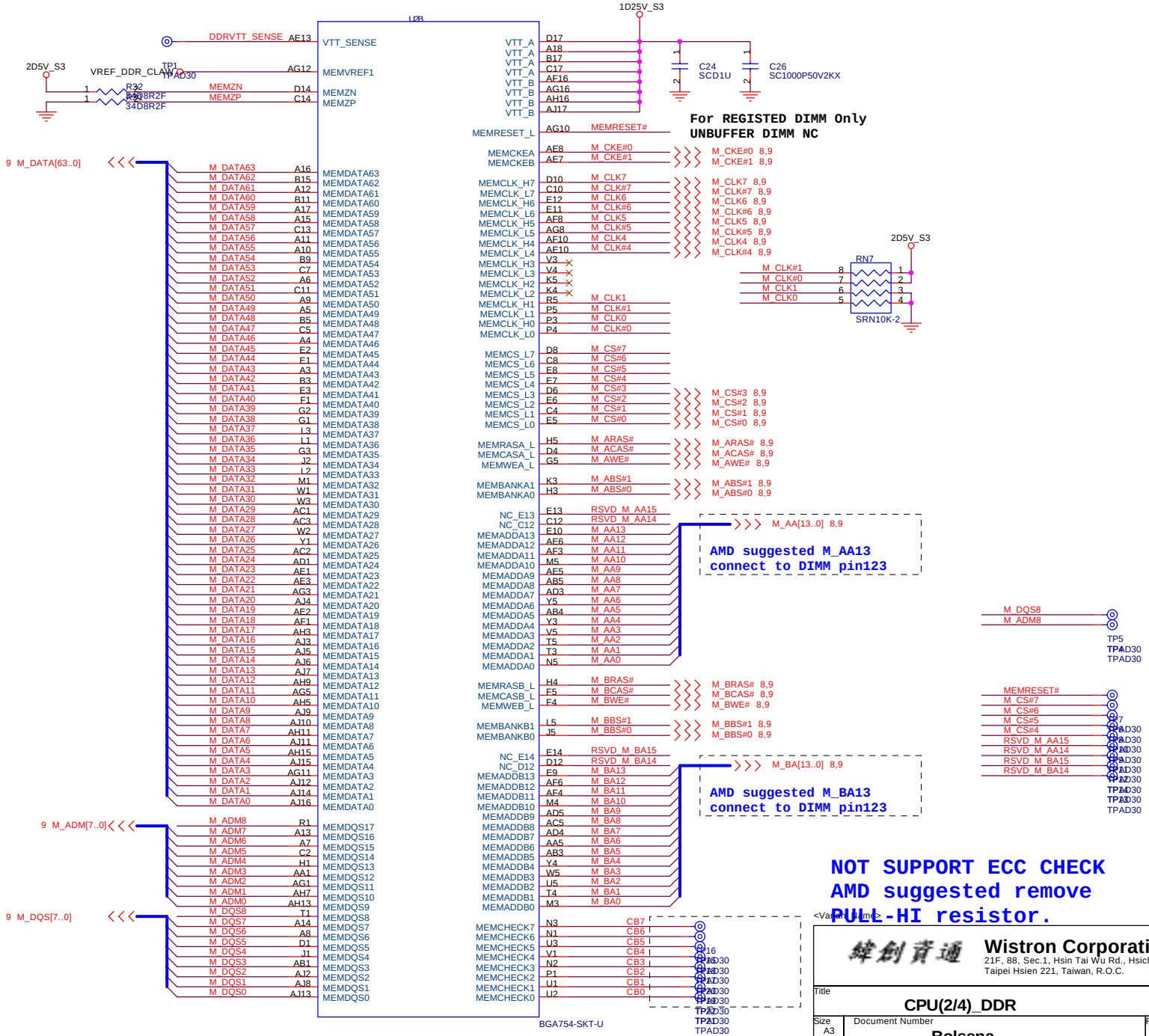
VREF_DDR_MEM



NOTE: Remove to bypass op-amp

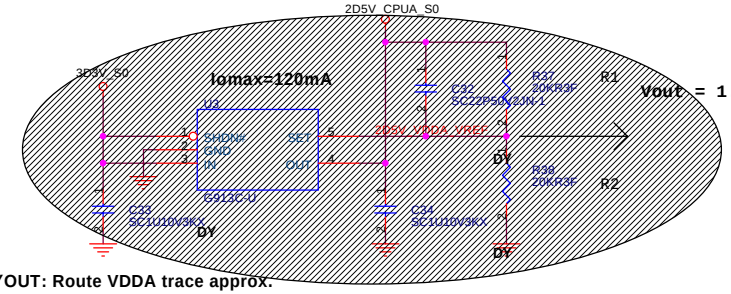
VREF_DDR_CLAW





蜂創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**CPU(2/4)_DDR**
Size A3	Document Number **Bolsena** Rev SA
Date: Tuesday, December 28, 2004	Sheet 5 of 58

2D5V_VDDA_S0



2D5V_S0

R39 0R3-U 2D5V_CPUR_S0

C35 SC10U10V5ZY

Change L270H

2D5V_VDDA_S0

AMD SUGGEST TO USE 100 ~ 300UH

2D5V_CPUA_S0

R40 0R3-U

R59 0R5J-1

63.R0004.151

TC1 ST100U4VBM-1

DY

C39 SC47U10V5ZY

LAYOUT: Route trace 50 mils wide and 500 to 750 mils long between these caps.

LAYOUT: Route VDDA trace approx. 50 mils wide (use 2x25 mil traces to exit ball field) and 500 mils long.

C36 SC3300P50V2KX

C40 SCD22U16V3ZY

1D2V_HT0B_S0

R44 44D2R3F

R42 44D2R3F

64.44R25.551

C37 SC1000P50V2KX

C41 SC1000P50V2KX

AMD SUGGEST TO USE 2D5V_CPUA_S0

KEMET,NT:5.7, B2 size
ST100U4VBM-1 (80.10716.321)
Iripple=1.1A,ESR=70mohm

SANYO, NT$:6.1
Iripple=1.1A,ESR=70mohm
3.5/2.8/2.0
77.21071.031

AMD suggest voltege from 2D5V_S0 to 2D5V_S3
differentially impedance 100

2D5V_S3

R46 820R3

R47 820R3

1D25V_S3

2D5V_S0

LDT_RST#
SB_CPUPWRGD
LDT_STP#

R48 680R3

R49 680R3

R50 680R3

2D5V_S0

R51 680R3

R52 680R3

2D5V_S0

C44 SCD1U

RN8 SRN680-U

R53 680R3

R54 680R3

DBREQ_J
DBRDY
TCK
TMS
TDI
TRST_L
TDO

DY

2D5V_S3

R57 680R3

CHANGE FROM 1KR3 TO 680R2 FOR AMD CHECK LIST

RN10 SRN680-U

NC_AG17
NC_AJ18
NC_D18

RN11 SRN680-U

NC_B19
NC_C19
NC_D20
NC_C21

U2C

VDDA1 AH25
VDDA2 AJ25

RESET_L AF20
PWROK AE18
LDTSTOP_L AJ27

L0_REF1 AF27
L0_REF0 AE26

COREFB A23
COREFB# A24
CORE_SENSE B23

VDDIOFB AE12
VDDIOFBJ AE12
VDDIOSENSE AE11

CLKIN AJ21
CLKIN_L AH21

CLKIN# AJ23
NC_AJ23 AH23
NC_AH23
NC_AE24 AE24
NC_AF24 AF24

VTT_A C16
VTT_B AG15

DBRDY AH17

NC_C15 C15

TMS E20
TCK E17
TRST_L B21
TDI A21

NC_C18 C18

NC_A19 A19

KEY1 A28
KEY0 AJ28

NC_AE23 AE23
NC_AF23 AF23
NC_AF22 AF22
NC_AF21 AF21

NC_C1 C1
NC_J3 J3
NC_R3 R3
NC_AA2 AA2
NC_D3 D3
NC_AG2 AG2
NC_B18 B18
NC_AH1 AH1
NC_AE21 AE21
NC_C20 C20
NC_AG4 AG4
NC_C6 C6
NC_AG6 AG6
NC_AE9 AE9
NC_AG9 AG9

THERMTRIP_L A20 THERMTRIP#

THERMDA A26
THERMDC A27

THERMDP 23
THERMDN 23
VID[4..0] 41

VID4 AG13 VID4
VID3 AF14 VID3
VID2 AG14 VID2
VID1 AF15 VID1
VID0 AE15 VID0

NC_AG18 AG18 NC_AG18
NC_AH18 AH18 NC_AH18
NC_AG17 AG17 NC_AG17
NC_AJ18 AJ18 NC_AJ18

TP23
TPAD30
TPAD30

FBCLKOUT_H AH19
FBCLKOUT_L AJ19

R47 80D6R3F-U

DBREQ_L AE19 DBREQJ

NC_D20 D20 NC_D20
NC_C21 C21 NC_C21
NC_D18 D18 NC_D18
NC_C19 C19 NC_C19
NC_B19 B19 NC_B19

TDO A22 TDO

NC_AF18 AF18 2D5V_S3

NC_D22 D22
NC_C22 C22

NC_B13 B13
NC_B7 B7
NC_C3 C3
NC_K1 K1
NC_R2 R2
NC_AA3 AA3
NC_F3 F3
NC_C23 C23
NC_AG7 AG7
NC_AE22 AE22
NC_C24 C24
NC_A25 A25
NC_C9 C9

BGA754-SKT-U

LAYOUT: Route FBCLKOUT_H/L differentially impedance 80

FBCLKOUT

FBCLKOUTJ

DY

Connect to VDDIO for AMD suggest.

2D5V_S0

R55 680R3

3D3V_S5

R56 10KR2

THERMTRIP#

Q1 MMBT3904-U1

CPU_THERMTRIP# 21,23

2D5V_S0

NS3

R58 1KR2

THERMTRIP#Level shift to SB400

Validation Test Points

LAYOUT: Place close to the CPU.

NC_C15
NC_AE23
NC_AF23
NC_AF22
NC_AF21

LDT_RST#
CLKIN
CLKIN#
CORE_SENSE
VDDIOFB
VDDIOFBJ
VDDIOSENSE
NC_AE24
NC_AF24

TPAD30

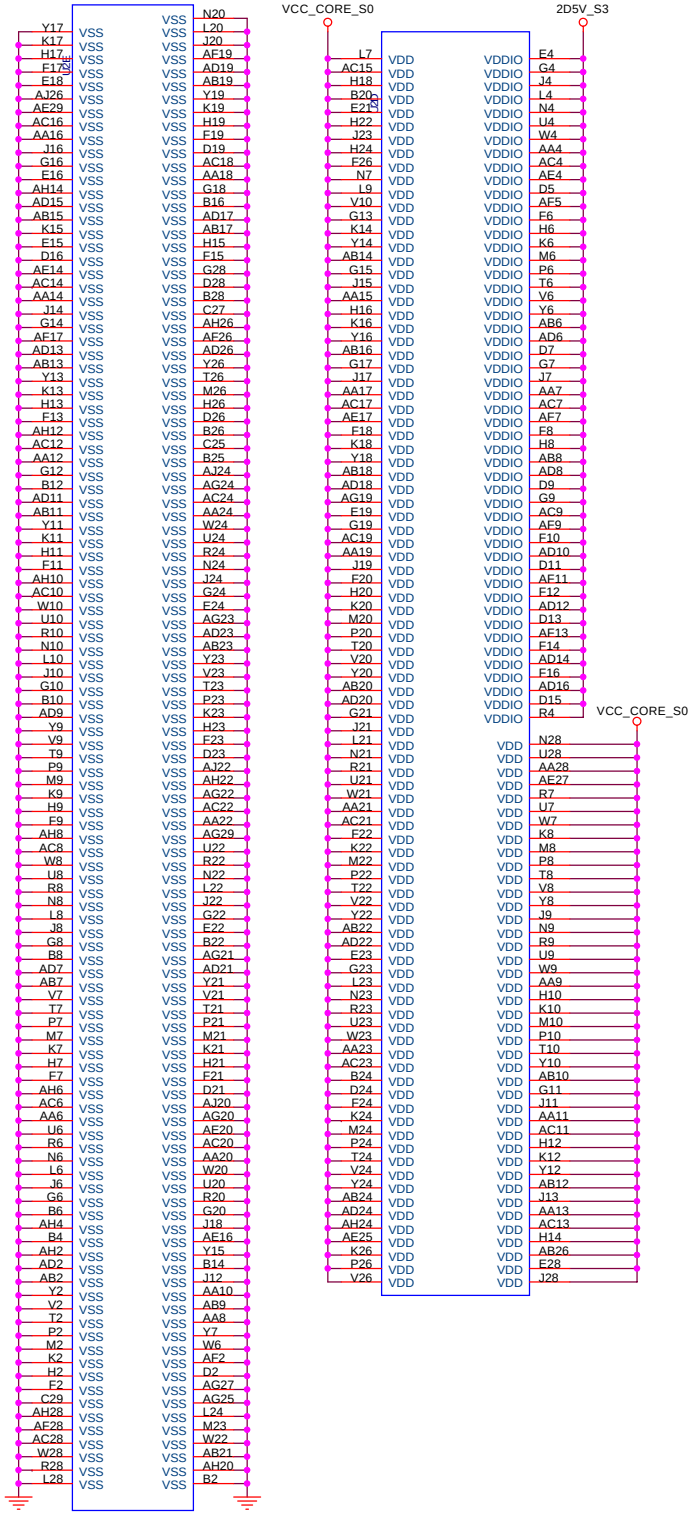
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

<Variant Name>

Title: CPU(3/4)_Control & Debug

Size: A3 | Document Number: Bolsena | Rev: SA

Date: Tuesday, December 28, 2004 | Sheet 6 of 58



BGA754-SKT-U

LAYOUT: Place in uPGA socket cavity.

BGA754-SKT-U

VCC_CORE_S0

0.22u x 6 — 10u x 4

C45 SCD22U16V3ZY, C46 SCD22U16V3ZY, C47 SCD22U16V3ZY, C48 SCD22U16V3ZY, C49 SCD22U16V3ZY, C50 SCD22U16V3ZY, C51 SCD10U10V5ZY, C52 SCD10U10V5ZY, C53 SCD10U10V5ZY, C54 SCD10U10V5ZY

LAYOUT: Place on backside of processor.

VCC_CORE_S0

C55 SCD22U16V3ZY, C56 SCD22U16V3ZY, C57 SCD22U16V3ZY, C58 SCD22U16V3ZY, C59 SCD10U10V5ZY, C60 SCD10U10V5ZY

0.22u x 4 — 10u x 2

DY DY DY DY

2D5V_S3

C61 SCD22U16V3ZY, C62 SCD22U16V3ZY, C63 SCD22U16V3ZY, C64 SCD22U16V3ZY, C65 SCD22U16V3ZY, C66 SCD22U16V3ZY

2D5V_S3

78.47593.411

C67 SC10U10V5ZY, C68 SC4D7U10V5ZY, C69 SC4D7U10V5ZY, C70 SC4D7U10V5ZY, C71 SC4D7U10V5ZY, C72 SC4D7U10V5ZY, C73 SC4D7U10V5ZY

10u x 1 — 4.7u x 6

1D25V_S3 — 1D25V_S3

C74 SCD22U16V3ZY, C75 SCD22U16V3ZY, C76 SC4D7U10V5ZY, C77 SC4D7U10V5ZY

0.22u x 2 — 4.7u x 2

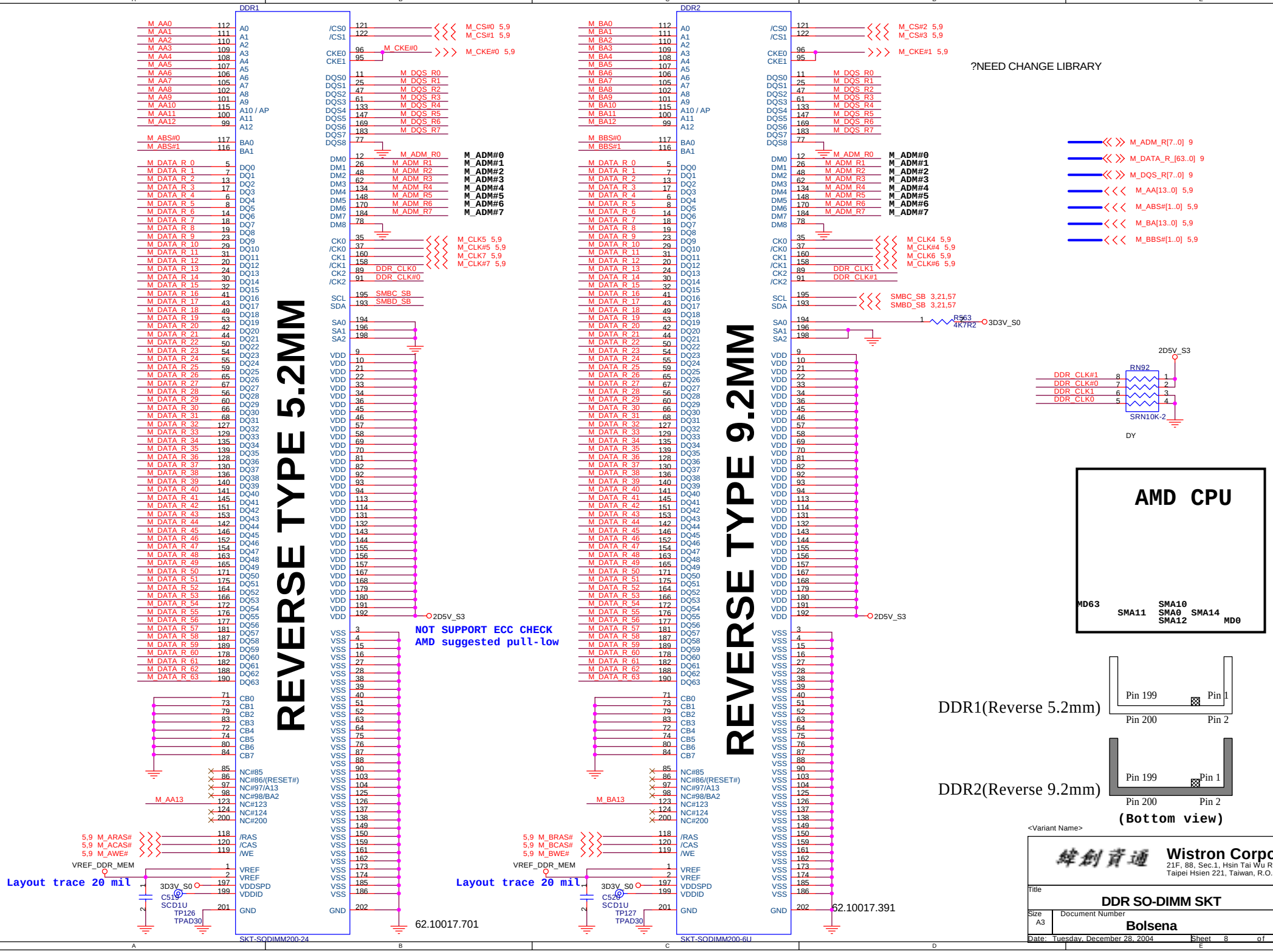
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(4/4)_Power

Size: A3 | Document Number: Bolsena | Rev: SA

Date: Tuesday, December 28, 2004 | Sheet 7 of 58


DDR1
REVERSE TYPE 5.2MM
SKT-SODIMM200-24
62.10017.701
NOT SUPPORT ECC CHECK
AMD suggested pull-low
Layout trace 20 mil
DDR2
REVERSE TYPE 9.2MM
SKT-SODIMM200-6U
62.10017.391
Layout trace 20 mil
?NEED CHANGE LIBRARY
M_ADM#0
M_ADM#1
M_ADM#2
M_ADM#3
M_ADM#4
M_ADM#5
M_ADM#6
M_ADM#7
2D5V_S3
3D3V_S0
RN92
SRN10K-2
DY
AMD CPU
MD63
SMA11
SMA10
SMA0
SMA14
SMA12
MD0
DDR1(Reverse 5.2mm)
Pin 199
Pin 1
Pin 200
Pin 2
DDR2(Reverse 9.2mm)
Pin 199
Pin 1
Pin 200
Pin 2
(Bottom view)
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDR SO-DIMM SKT
Size
A3
Document Number
Bolsena
Rev
SA
Date: Tuesday, December 28, 2004
Sheet 8 of 58

SERIES DAMPING

PLACE RNs CLOSE TO FIRST DIMM, < 0.75"
STRICT EQUAL LENGTH LIMITATION WITH DQS,
CB PINS

SRN10J-3 — RN13

M_DATA4	8	9	M_DATA_R_4
M_DATA5	7	10	M_DATA_R_5
M_ADM0	6	11	M_ADM_R0
M_DATA6	5	12	M_DATA_R_6
M_DATA7	4	13	M_DATA_R_7
M_DATA13	3	14	M_DATA_R_13
M_DATA12	2	15	M_DATA_R_12
M_ADM1	1	16	M_ADM_R1

SRN10J-3 — RN14

M_DATA32	8	9	M_DATA_R_32
M_DATA33	7	10	M_DATA_R_33
M_DATA36	6	11	M_DATA_R_36
M_DATA37	5	12	M_DATA_R_37
M_DQS4	4	13	M_DQS_R4
M_ADM4	3	14	M_ADM_R4
M_DATA34	2	15	M_DATA_R_34
M_DATA39	1	16	M_DATA_R_39

SRN10J-3 — RN18

M_DATA1	8	9	M_DATA_R_1
M_DATA0	7	10	M_DATA_R_0
M_DQS0	6	11	M_DQS_R0
M_DATA2	5	12	M_DATA_R_2
M_DATA3	4	13	M_DATA_R_3
M_DATA8	3	14	M_DATA_R_8
M_DATA9	2	15	M_DATA_R_9
M_DQS1	1	16	M_DQS_R1

SRN10J-3 — RN19

M_DATA35	8	9	M_DATA_R_35
M_DATA41	7	10	M_DATA_R_41
M_DATA40	6	11	M_DATA_R_40
M_DQS5	5	12	M_DQS_R5
M_DATA42	4	13	M_DATA_R_42
M_DATA43	3	14	M_DATA_R_43
M_DATA49	2	15	M_DATA_R_49
M_DATA48	1	16	M_DATA_R_48

SRN10J-3 — RN24

M_DATA14	8	9	M_DATA_R_14
M_DATA15	7	10	M_DATA_R_15
M_DATA21	6	11	M_DATA_R_21
M_DATA20	5	12	M_DATA_R_20
M_ADM2	4	13	M_ADM_R2
M_DATA23	3	14	M_DATA_R_23
M_DATA22	2	15	M_DATA_R_22
M_DATA25	1	16	M_DATA_R_25

SRN10J-3 — RN25

M_DATA38	8	9	M_DATA_R_38
M_DATA45	7	10	M_DATA_R_45
M_DATA44	6	11	M_DATA_R_44
M_ADM5	5	12	M_ADM_R5
M_DATA47	4	13	M_DATA_R_47
M_DATA46	3	14	M_DATA_R_46
M_DATA53	2	15	M_DATA_R_53
M_DATA52	1	16	M_DATA_R_52

SRN10J-3 — RN29

M_DATA11	8	9	M_DATA_R_11
M_DATA10	7	10	M_DATA_R_10
M_DATA17	6	11	M_DATA_R_17
M_DATA16	5	12	M_DATA_R_16
M_DQS2	4	13	M_DQS_R2
M_DATA19	3	14	M_DATA_R_19
M_DATA18	2	15	M_DATA_R_18
M_DATA24	1	16	M_DATA_R_24

SRN10J-3 — RN30

M_DQS6	8	9	M_DQS_R6
M_DATA50	7	10	M_DATA_R_50
M_DATA51	6	11	M_DATA_R_51
M_DATA56	5	12	M_DATA_R_56
M_DATA57	4	13	M_DATA_R_57
M_DQS7	3	14	M_DQS_R7
M_DATA58	2	15	M_DATA_R_58
M_DATA59	1	16	M_DATA_R_59

SRN10J-3 — RN34

M_DATA29	8	9	M_DATA_R_29
M_DATA28	7	10	M_DATA_R_28
M_DQS3	6	11	M_DQS_R3
M_ADM3	5	12	M_ADM_R3
M_DATA26	4	13	M_DATA_R_26
M_DATA27	3	14	M_DATA_R_27
M_DATA30	2	15	M_DATA_R_30
M_DATA31	1	16	M_DATA_R_31

SRN10J-3 — RN35

M_ADM6	8	9	M_ADM_R6
M_DATA54	7	10	M_DATA_R_54
M_DATA55	6	11	M_DATA_R_55
M_DATA61	5	12	M_DATA_R_61
M_DATA60	4	13	M_DATA_R_60
M_ADM7	3	14	M_ADM_R7
M_DATA62	2	15	M_DATA_R_62
M_DATA63	1	16	M_DATA_R_63

5,8 M_CKE#0 — M_CKE#0

5,8 M_CKE#1 — M_CKE#1

05/10
Remove the damping resistor for AMD suggest.

PARALLEL TERMINATION

PULL HIGH STUBS < 0.8", PLACE RPs CLOSE TO SECOND DM (DM2)
NO EQUAL LENGTH LIMITATION

1D25V_S3

SRN68J-1 — RN15

M_ADM_R1	8	9	
M_DATA_R_13	7	10	
M_DATA_R_12	6	11	
M_DATA_R_7	5	12	
M_DATA_R_6	4	13	
M_ADM_R0	3	14	
M_DATA_R_5	2	15	
M_DATA_R_4	1	16	

SRN68J-1 — RN16

	8	9	M_DATA_R_32
	7	10	M_DATA_R_33
	6	11	M_DATA_R_36
	5	12	M_DATA_R_37
	4	13	M_ADM_R4
	3	14	M_DQS_R4
	2	15	M_DATA_R_38
	1	16	M_DATA_R_39

SRN68J-1 — RN20

M_DATA_R_1	8	9	
M_DATA_R_0	7	10	
M_DQS_R0	6	11	
M_DATA_R_2	5	12	
M_DATA_R_3	4	13	
M_DATA_R_8	3	14	
M_DATA_R_9	2	15	
M_DQS_R1	1	16	

SRN68J-1 — RN21

	8	9	M_DATA_R_48
	7	10	M_DATA_R_49
	6	11	M_DATA_R_43
	5	12	M_DATA_R_42
	4	13	M_DQS_R5
	3	14	M_DATA_R_41
	2	15	M_DATA_R_40
	1	16	M_DATA_R_34

SRN68J-1 — RN26

M_DATA_R_25	8	9	
M_DATA_R_23	7	10	
M_DATA_R_22	6	11	
M_ADM_R2	5	12	
M_DATA_R_21	4	13	
M_DATA_R_20	3	14	
M_DATA_R_15	2	15	
M_DATA_R_14	1	16	

SRN68J-1 — RN27

	8	9	M_DATA_R_35
	7	10	M_DATA_R_44
	6	11	M_DATA_R_45
	5	12	M_ADM_R5
	4	13	M_DATA_R_46
	3	14	M_DATA_R_47
	2	15	M_DATA_R_52
	1	16	M_DATA_R_53

SRN68J-1 — RN31

M_DATA_R_11	8	9	
M_DATA_R_10	7	10	
M_DATA_R_16	6	11	
M_DATA_R_17	5	12	
M_DQS_R2	4	13	
M_DATA_R_19	3	14	
M_DATA_R_18	2	15	
M_DATA_R_24	1	16	

SRN68J-1 — RN32

	8	9	M_DATA_R_59
	7	10	M_DATA_R_58
	6	11	M_DQS_R7
	5	12	M_DATA_R_57
	4	13	M_DATA_R_56
	3	14	M_DATA_R_51
	2	15	M_DATA_R_50
	1	16	M_DQS_R6

SRN68J-1 — RN36

M_DATA_R_31	8	9	
M_DATA_R_30	7	10	
M_DATA_R_26	6	11	
M_DATA_R_27	5	12	
M_ADM_R3	4	13	
M_DQS_R3	3	14	
M_DATA_R_29	2	15	
M_DATA_R_28	1	16	

SRN68J-1 — RN37

	8	9	M_ADM_R6
	7	10	M_DATA_R_54
	6	11	M_DATA_R_55
	5	12	M_DATA_R_60
	4	13	M_DATA_R_61
	3	14	M_ADM_R7
	2	15	M_DATA_R_62
	1	16	M_DATA_R_63

1D25V_S3

SRN47J — RN22

M_CKE#0	1	4	
M_CKE#1	2	3	

RN17 SRN47J — RN23

M_BA12	1	4	
M_AA12	2	3	

SRN47J-1-U — RN28

M_AA11	8	9	
M_AA9	7	10	
M_AA7	6	11	
M_AA5	5	12	
M_AA4	4	13	
M_AA8	3	14	
M_AA6	2	15	
M_AA3	1	16	

RN23 SRN47J-1-U — RN33

M_CS#3	8	9	
M_BCAS#	7	10	
M_BRAS#	6	11	
M_BBS#1	5	12	
M_CS#2	4	13	
M_BA13	3	14	
M_BA0	2	15	
M_BA2	1	16	

RN28 SRN47J-1-U — RN38

M_AA1	8	9	
M_AA10	7	10	
M_AA2	6	11	
M_AA0	5	12	
M_ABS#1	4	13	
M_ARAS#	3	14	
M_AWE#	2	15	
M_ABS#0	1	16	

RN33 SRN47J-1-U — RN39 SRN47-1

M_BA7	8	9	
M_BA3	7	10	
M_BA6	6	11	
M_BA9	5	12	
M_BA10	4	13	
M_BA1	3	14	
M_BBS#0	2	15	
M_BWE#	1	16	

RN38 SRN47-1 — RN40 SRN47-1

M_BA4	4	5	
M_BA8	3	6	
M_BA11	2	7	
M_BA5	1	8	

M_AA13	4	5	
M_CS#0	3	6	
M_ACAS#	2	7	
M_CS#1	1	8	

M_ADM_R[7..0] 8
M_ADM[7..0] 5
M_DATA[63..0] 5
M_DATA_R_[63..0] 8
M_DQS[7..0] 5
M_DQS_R[7..0] 8
M_AA[13..0] 5,8
M_ABS#[1..0] 5,8
M_BA[13..0] 5,8
M_BBS#[1..0] 5,8

M_AWE# 5,8
M_ACAS# 5,8
M_ARAS# 5,8

M_BWE# 5,8
M_BCAS# 5,8
M_BRAS# 5,8

M_CS#0 5,8
M_CS#1 5,8
M_CS#2 5,8
M_CS#3 5,8

Place it near CPU

1	R60 121R3F	M_CLK7 / M_CLK#7	M_CLK7 5,8 / M_CLK#7 5,8
1	R61 121R3F	M_CLK6 / M_CLK#6	M_CLK6 5,8 / M_CLK#6 5,8
1	R62 121R3F	M_CLK5 / M_CLK#5	M_CLK5 5,8 / M_CLK#5 5,8
1	R63 121R3F	M_CLK4 / M_CLK#4	M_CLK4 5,8 / M_CLK#4 5,8

<Variant Name>

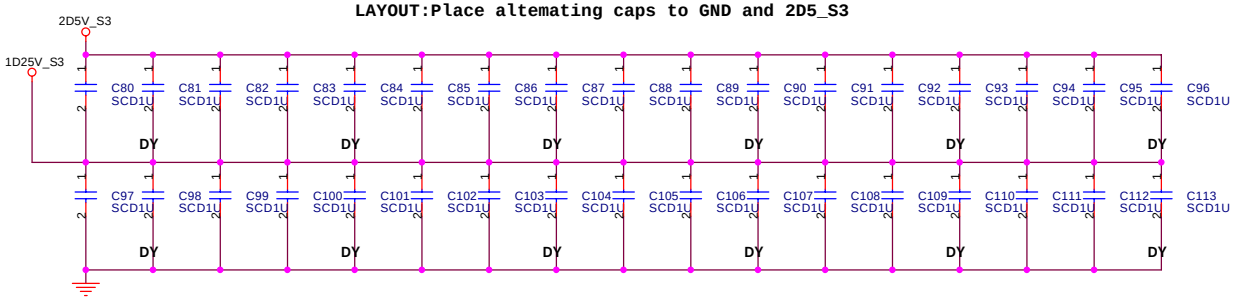
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

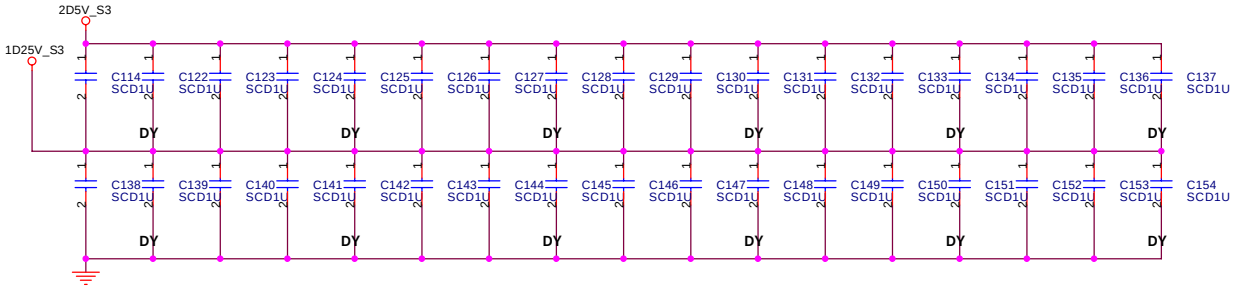
Title: **DDR DAMPING & TERMINATION**

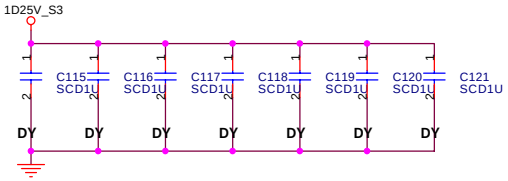
Size	Document Number	Rev
A3	**Bolsena**	SA

Date: Tuesday, December 28, 2004 Sheet 9 of 58

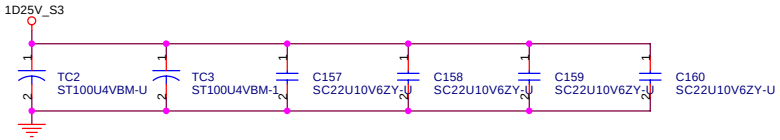
LAYOUT:Place altemating caps to GND and 2D5_S3



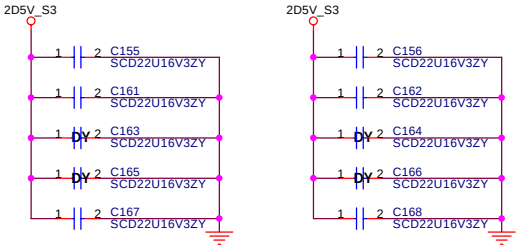




LAYOUT:Place at end of the DIMMs



LAYOUT:Place close to Power Pin of DDR socket.



0.22u x 10

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

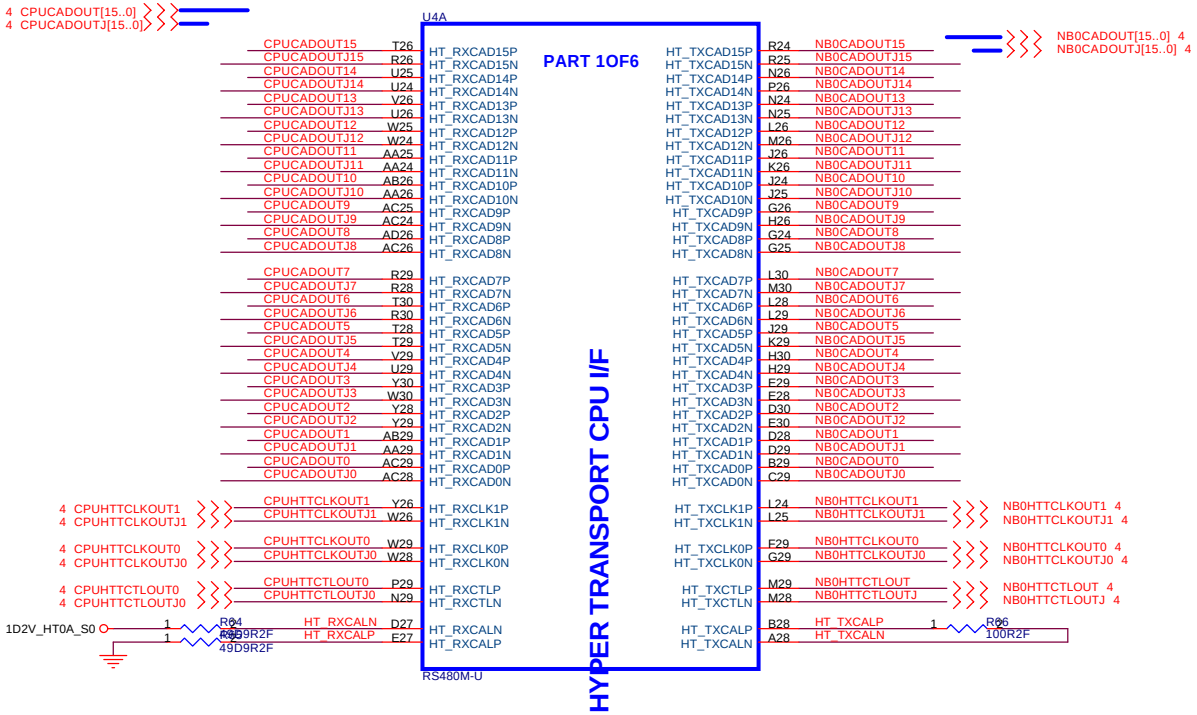
Title: **DDR DECOUPLING**

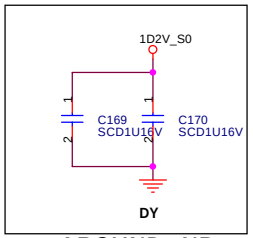
Size	Document Number	Rev
A3	**Bolsena**	SA

Date: Tuesday, December 28, 2004 Sheet 10 of 58

CLAW HAMMER TO NB

NB TO CLAW HAMMER





AROUND NB

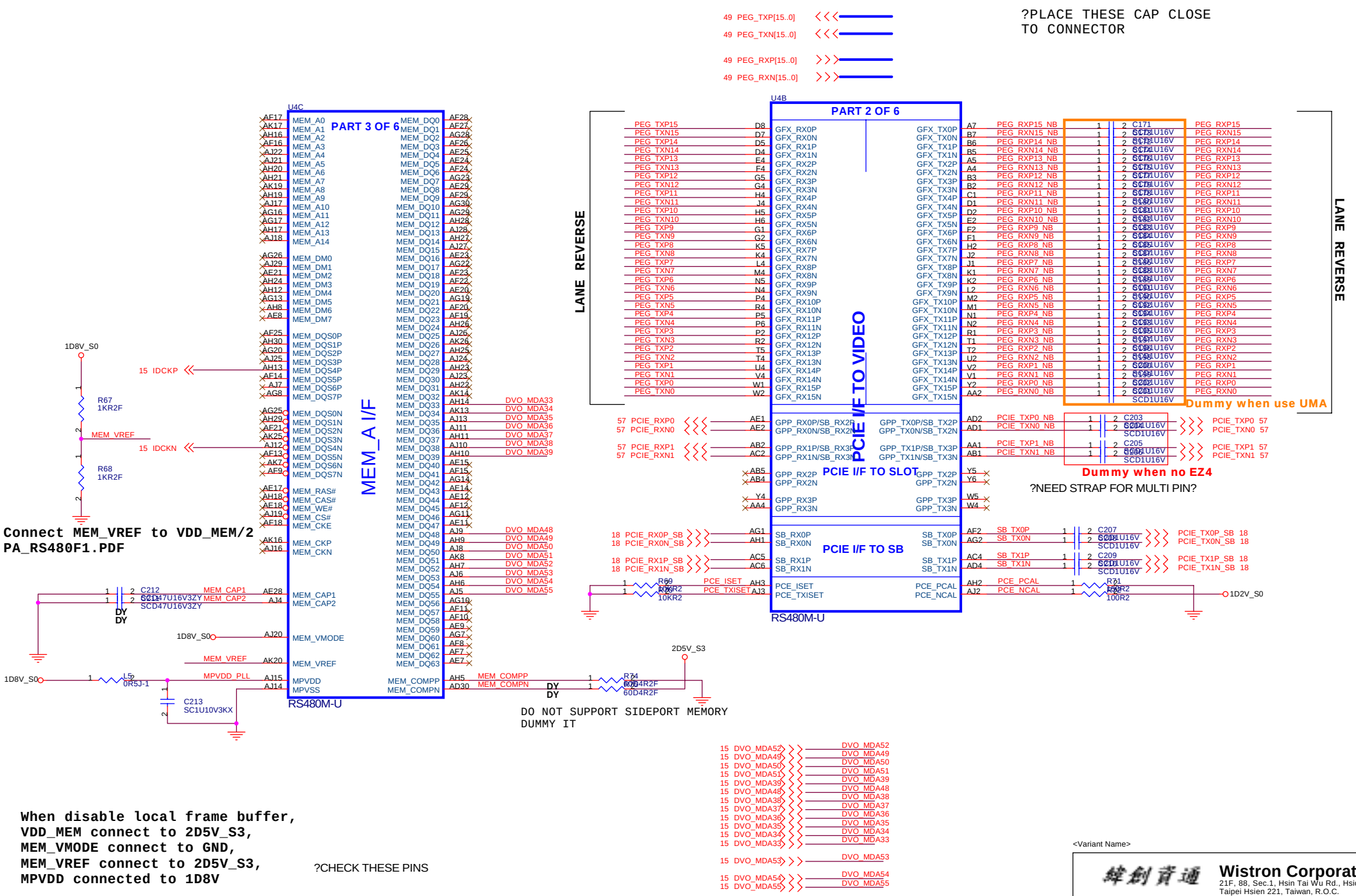
<Variant Name>

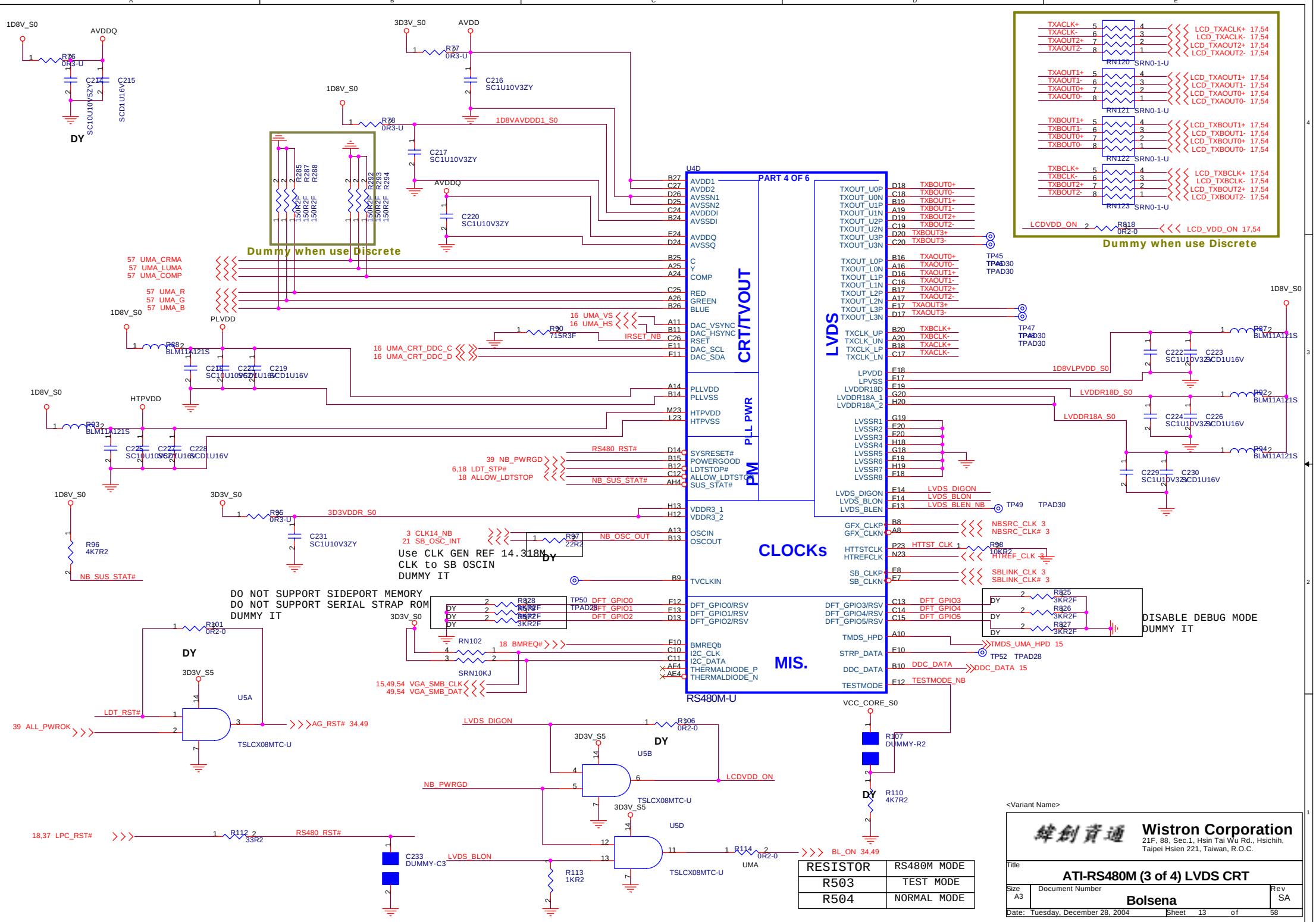
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

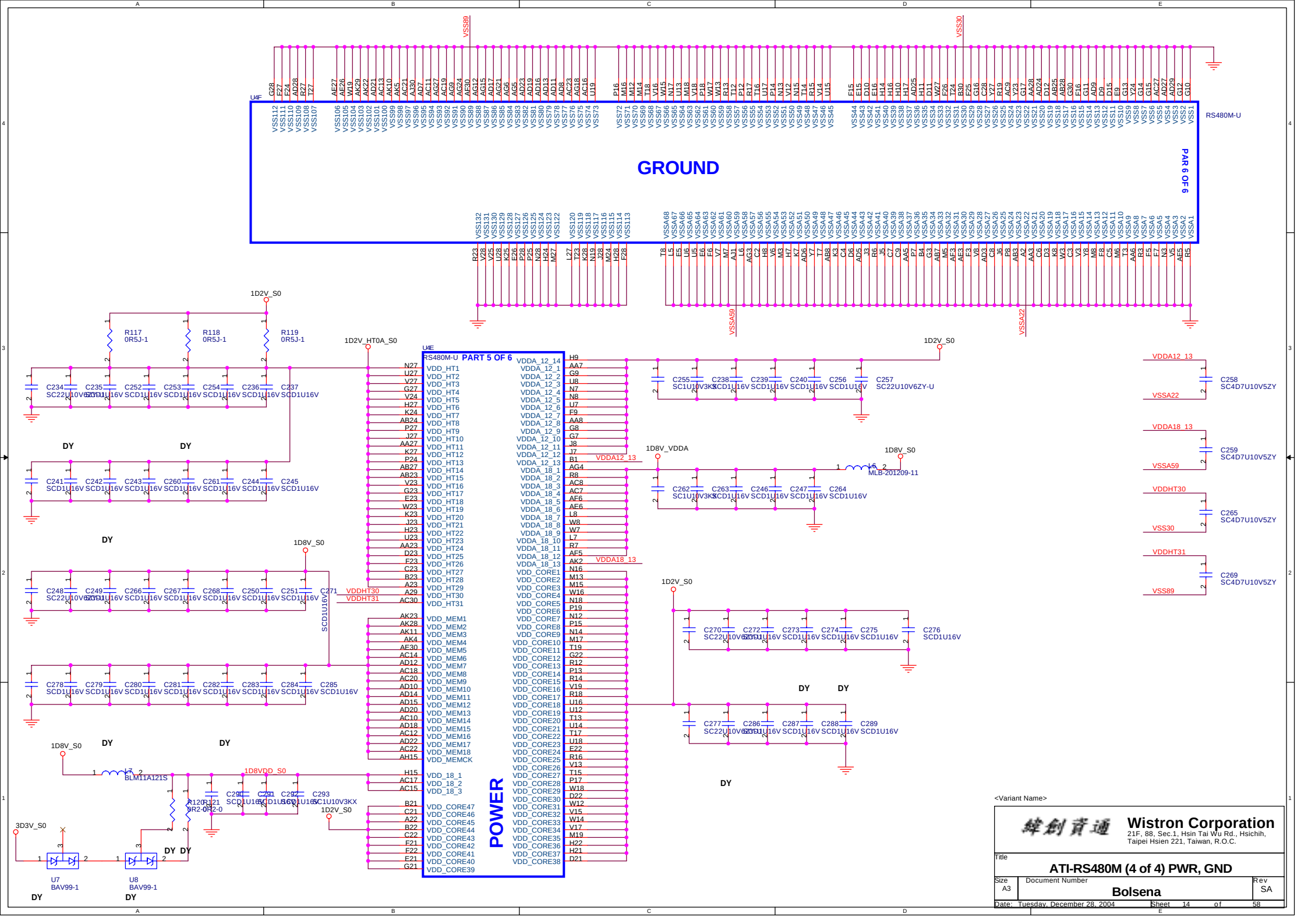
Title: ATI-RS480M (1 of 4) HT

Size: A3 | Document Number: Bolsena | Rev: SA

Date: Tuesday, December 28, 2004 | Sheet 11 of 58


?PLACE THESE CAP CLOSE TO CONNECTOR
49 PEG_TXP[15..0]
49 PEG_TXN[15..0]
49 PEG_RXP[15..0]
49 PEG_RXN[15..0]
U4C
PART 3 OF 6
MEM_A I/F
RS480M-U
U4B
PART 2 OF 6
PCIE I/F TO VIDEO
PCIE I/F TO SLOT
PCIE I/F TO SB
RS480M-U
LANE REVERSE
LANE REVERSE
Dummy when use UMA
Dummy when no EZ4
?NEED STRAP FOR MULTI PIN?
Connect MEM_VREF to VDD_MEM/2
PA_RS480F1.PDF
DO NOT SUPPORT SIDEPORT MEMORY
DUMMY IT
When disable local frame buffer,
VDD_MEM connect to 2D5V_S3,
MEM_VMODE connect to GND,
MEM_VREF connect to 2D5V_S3,
MPVDD connected to 1D8V
?CHECK THESE PINS
DSG-215-RS480-04.PDF
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATI-RS480M (2 of 4) PCIE
Size A3
Document Number
Bolsena
Rev SA
Date: Tuesday, December 28, 2004
Sheet 12 of 58


U4D
PART 4 OF 6
AVDD1
AVDD2
AVSSN1
AVSSN2
AVDDDI
AVSSDI
AVDDQ
AVSSQ
C
Y
COMP
RED
GREEN
BLUE
DAC_VSYNC
DAC_HSYNC
RSET
DAC_SCL
DAC_SDA
CRT/TVOUT
PLLVDD
PLLVSS
HTPVDD
HTPVSS
PLL PWR
SYSRESET#
POWERGOOD
LDTSTOP#
ALLOW_LDTSTOP
SUS_STAT#
PM
VDDR3_1
VDDR3_2
OSCIN
OSCOUT
TVCLKIN
CLOCKs
DFT_GPIO0/RSV
DFT_GPIO1/RSV
DFT_GPIO2/RSV
BMREQb
I2C_CLK
I2C_DATA
THERMALDIODE_P
THERMALDIODE_N
MIS.
RS480M-U
TXOUT_U0P
TXOUT_U0N
TXOUT_U1P
TXOUT_U1N
TXOUT_U2P
TXOUT_U2N
TXOUT_U3P
TXOUT_U3N
TXOUT_L0P
TXOUT_L0N
TXOUT_L1P
TXOUT_L1N
TXOUT_L2P
TXOUT_L2N
TXOUT_L3P
TXOUT_L3N
TXCLK_UP
TXCLK_UN
TXCLK_LP
TXCLK_LN
LVDS
LPVDD
LPVSS
LVDDR18D
LVDDR18A_1
LVDDR18A_2
LVSSR1
LVSSR2
LVSSR3
LVSSR4
LVSSR5
LVSSR6
LVSSR7
LVSSR8
LVDS_DIGON
LVDS_BLON
LVDS_BLEN
GFX_CLKP
GFX_CLKN
HTTSTCLK
HTREFCLK
SB_CLKP
SB_CLKN
DFT_GPIO3/RSV
DFT_GPIO4/RSV
DFT_GPIO5/RSV
TMDS_HPD
STRP_DATA
DDC_DATA
TESTMODE
Dummy when use Discrete
Use CLK GEN REF 14.318M
CLK to SB OSCIN
DUMMY IT
DO NOT SUPPORT SIDEPORT MEMORY
DO NOT SUPPORT SERIAL STRAP ROM
DUMMY IT
DISABLE DEBUG MODE
DUMMY IT
TSLCX08MTC-U
SRN10KJ
VCC_CORE_S0
R107
DUMMY-R2
R110
4K7R2
LCDVDD_ON
BL_ON 34,49
RESISTOR
R503
R504
TEST MODE
NORMAL MODE
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATI-RS480M (3 of 4) LVDS CRT
Size
A3
Document Number
Bolsena
Rev
SA
Date: Tuesday, December 28, 2004
Sheet 13 of 58



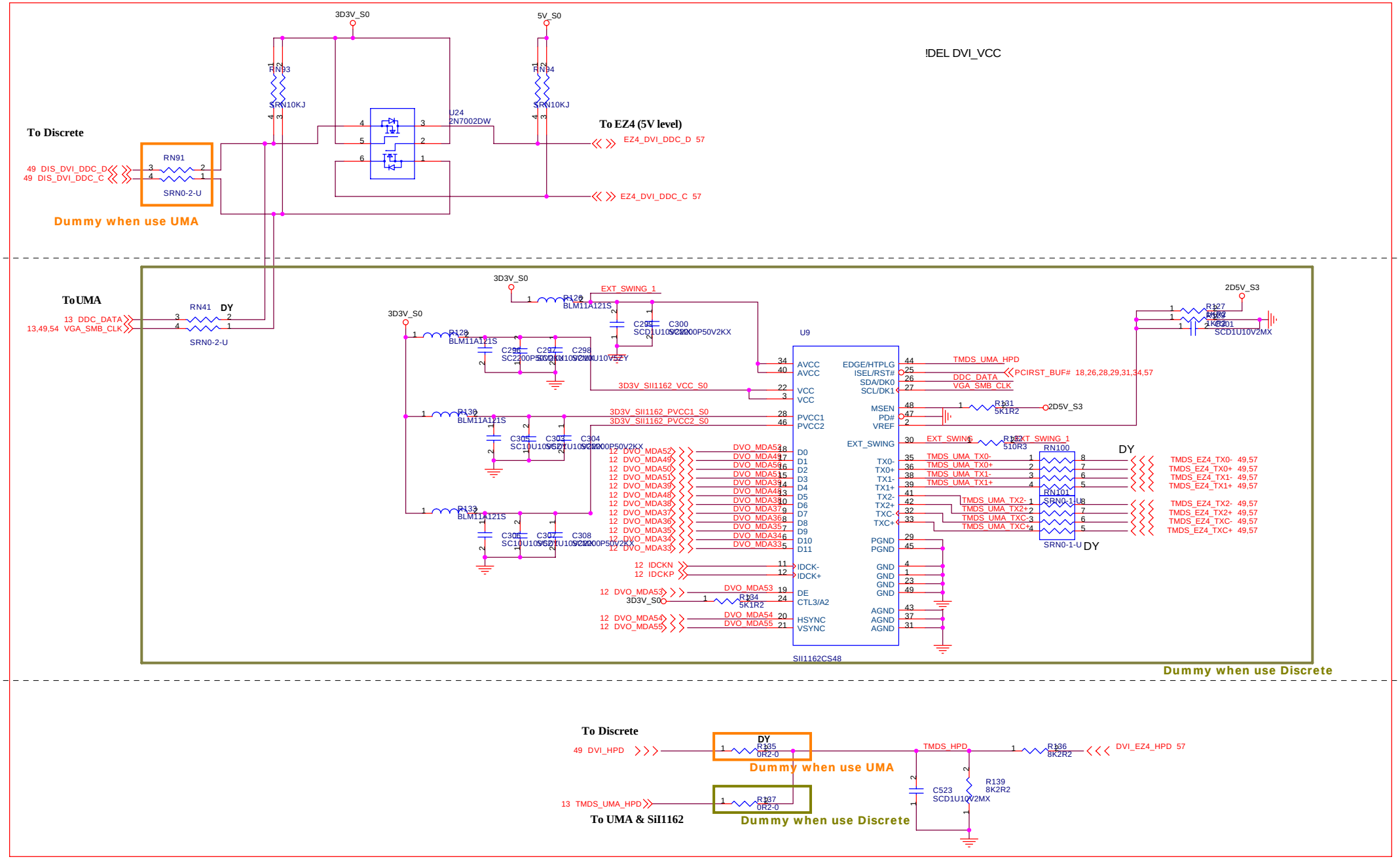
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

<Variant Name>

Title: ATI-RS480M (4 of 4) PWR, GND

Size: A3 | Document Number: Bolsena | Rev: SA

Date: Tuesday, December 28, 2004 | Sheet 14 of 58



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

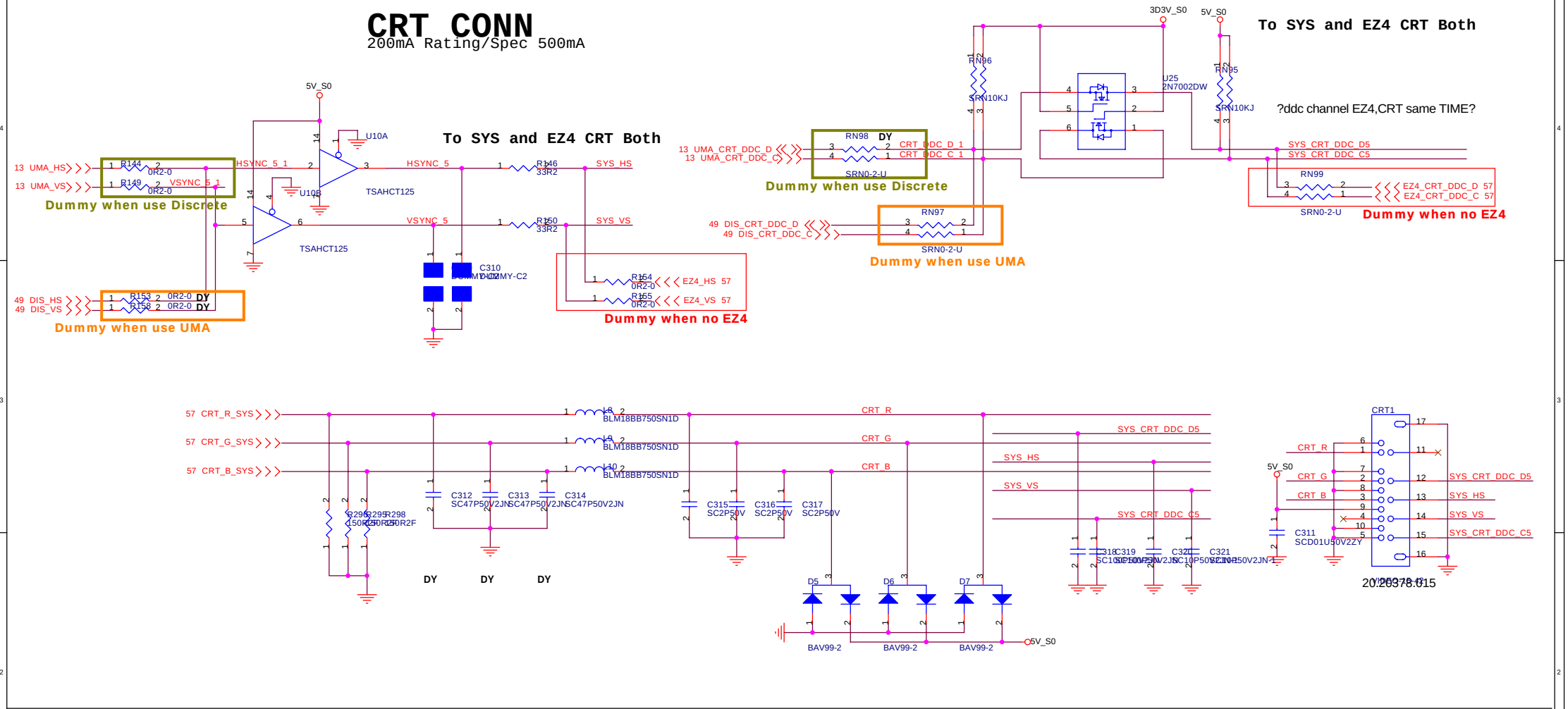
Title: **UMA DVI - SiI 1162**

Size: A3 | Document Number: **Bolsena** | Rev: SA

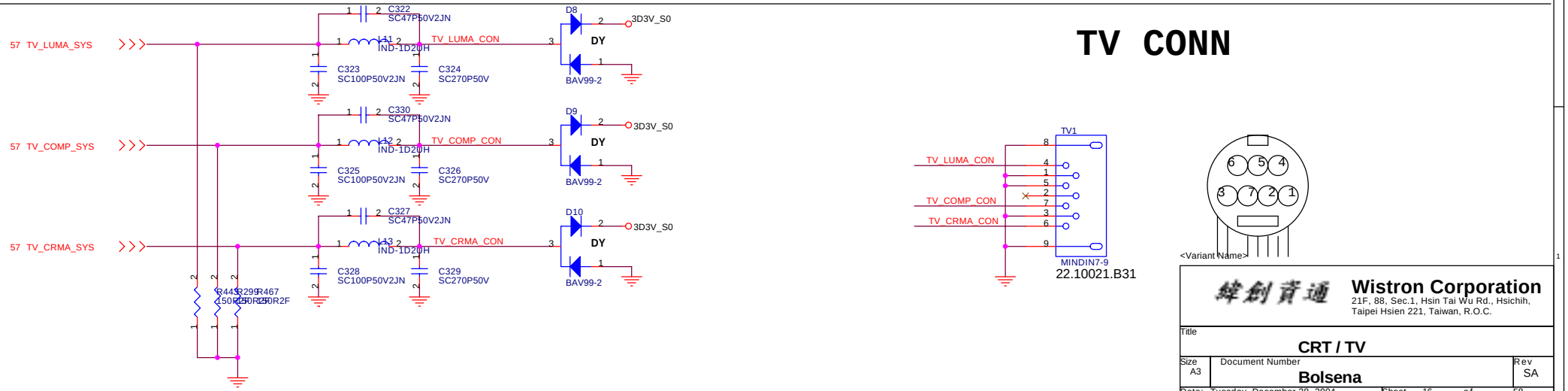
Date: Tuesday, December 28, 2004 | Sheet 15 of 58

CRT CONN

200mA Rating/Spec 500mA

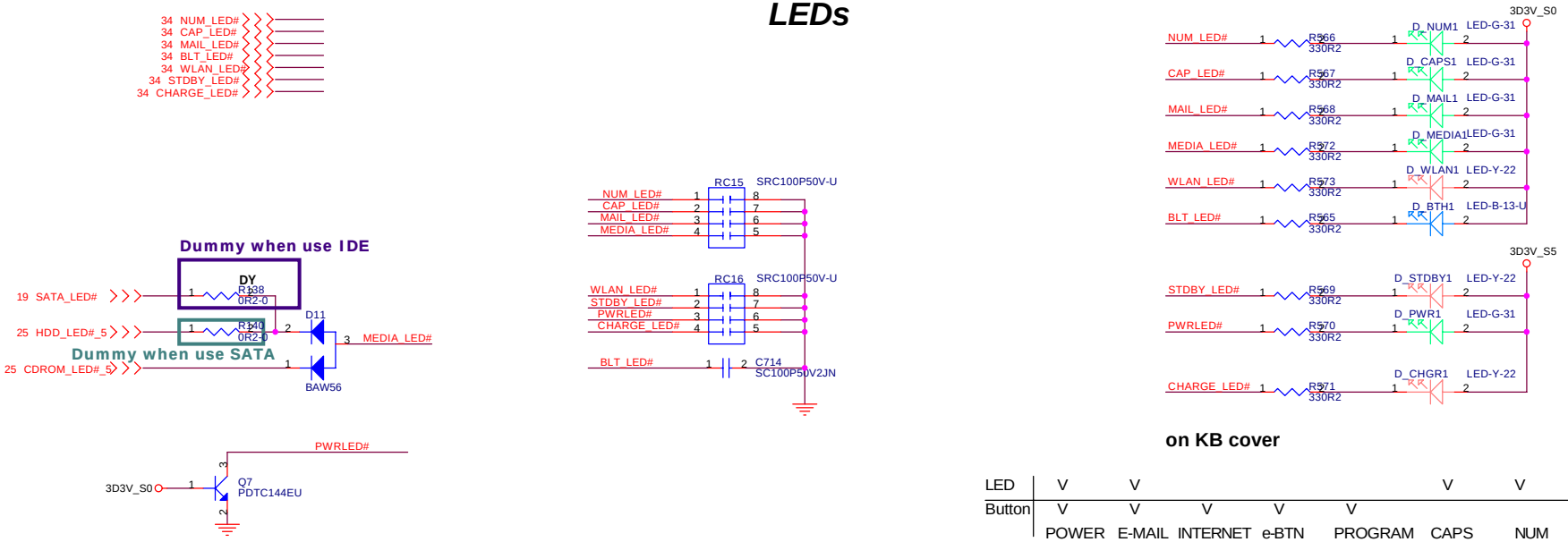


TV CONN



蜂創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**CRT / TV**	
Size A3	Document Number **Bolsena**	Rev SA
Date: Tuesday, December 28, 2004	Sheet 16 of 58	

LEDs



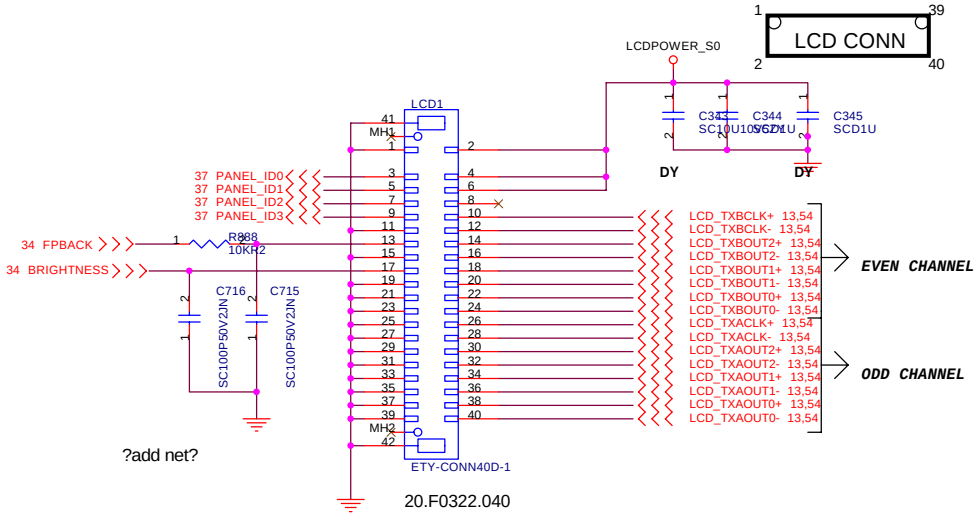
on KB cover

LED	V	V				V	V	V
Button	V	V	V	V	V			
	POWER	E-MAIL	INTERNET	e-BTN	PROGRAM	CAPS	NUM	HDD

Front panel

LED	V	V	V	V
Button	V	V		
	BlutTooth	WirelessCharger		Power

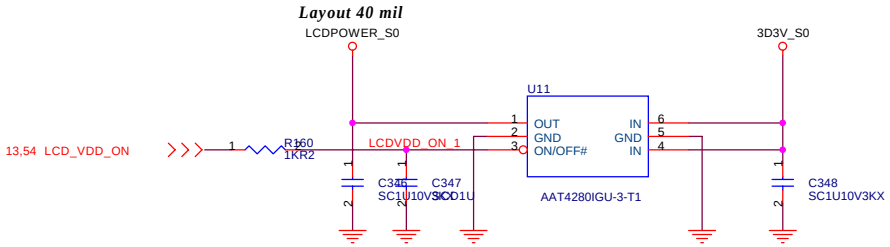
LCD CONN



?add net?

20.F0322.040

LCD POWER



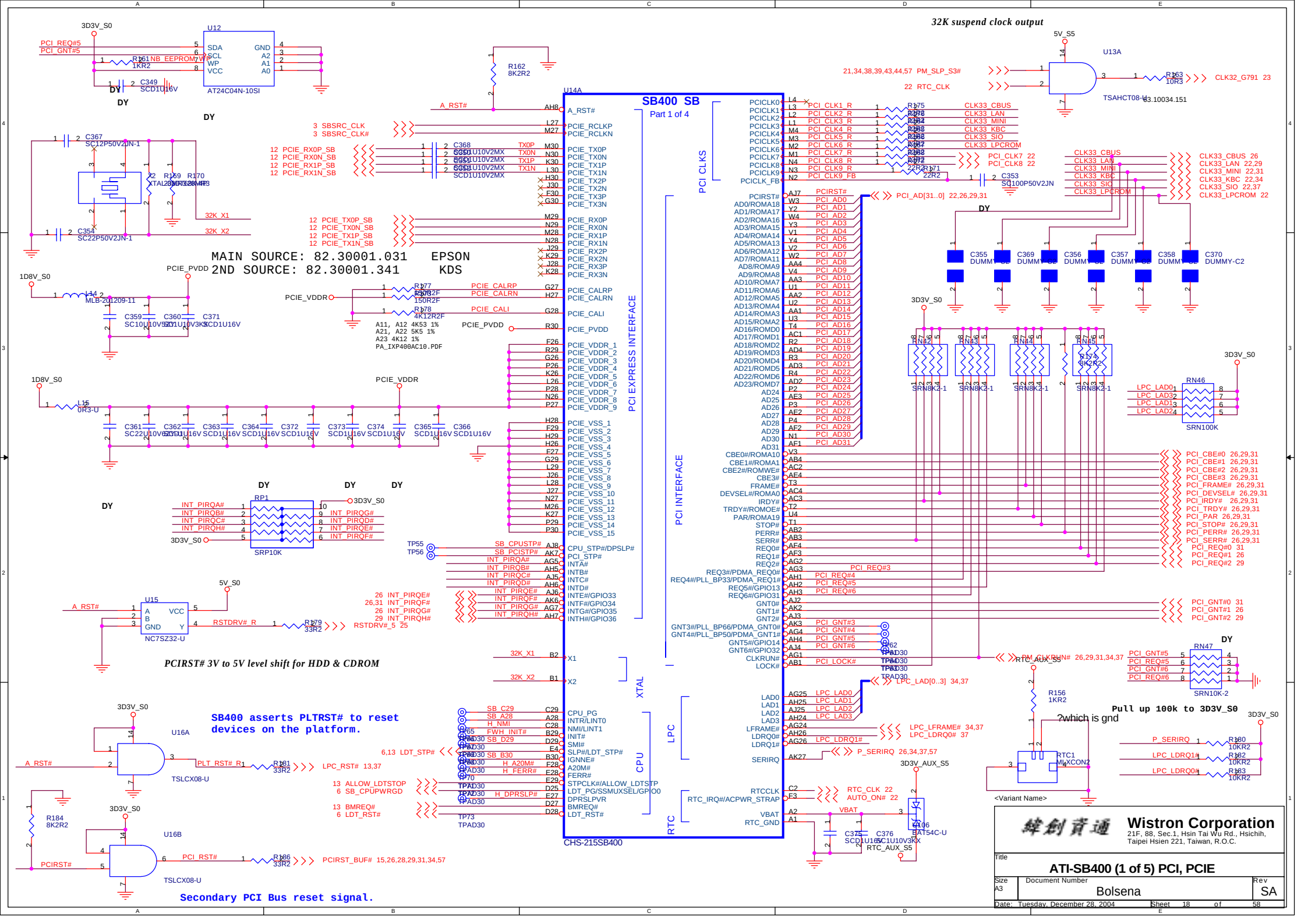
<Variant Name>

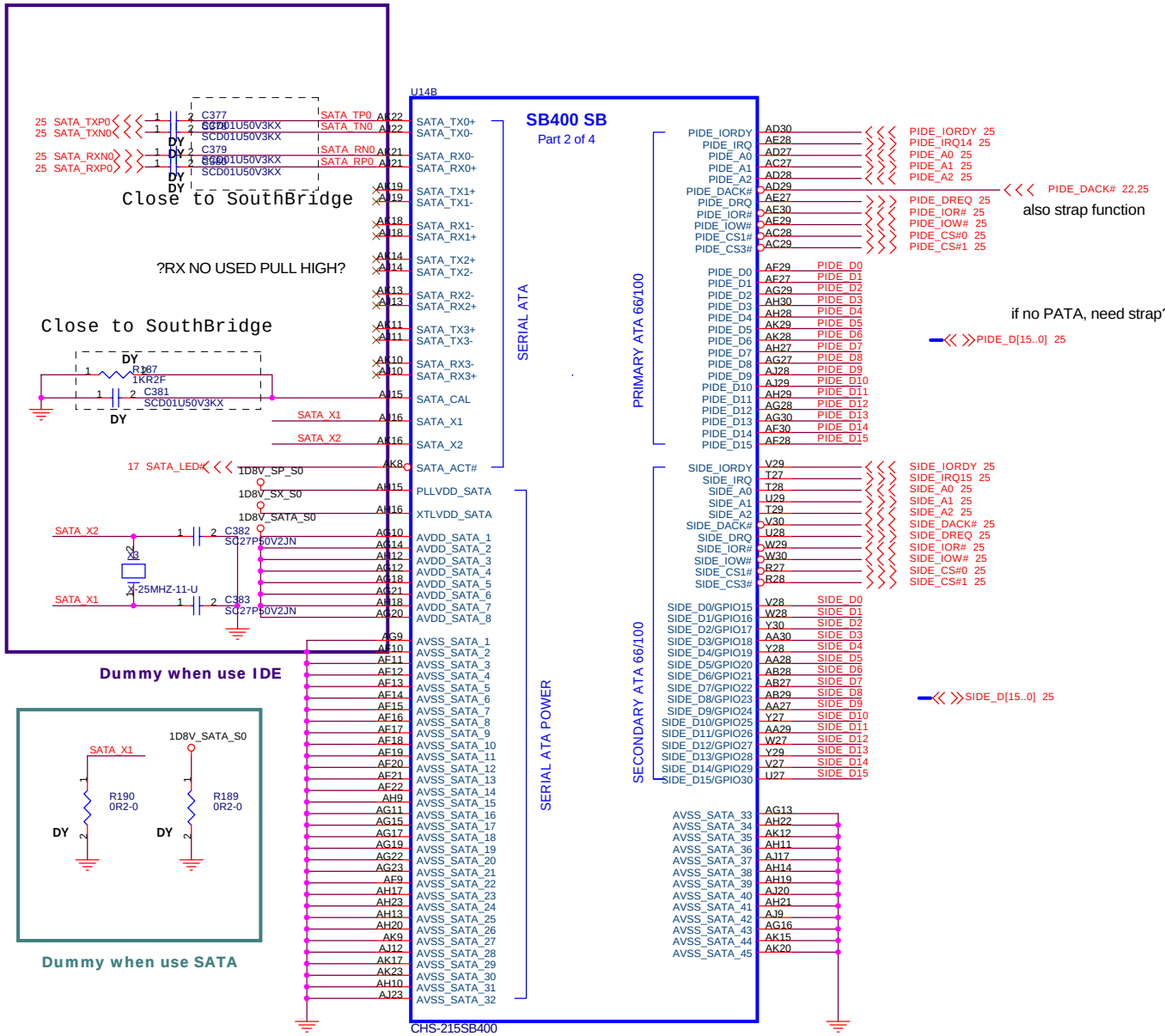
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

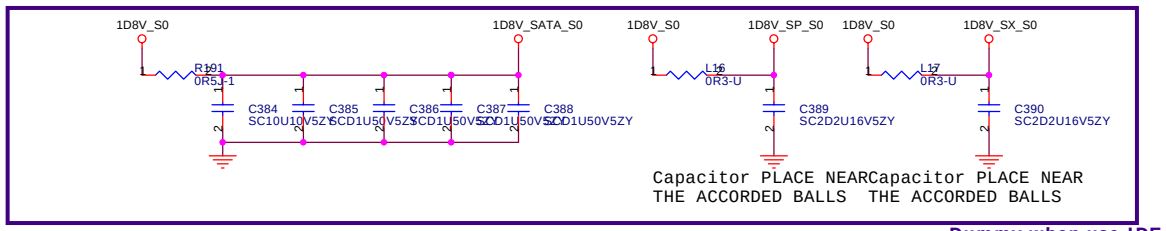
Title: **INV / LCD / LEDs**

Size: A3 | Document Number: **Bolsena** | Rev: SA

Date: Tuesday, December 28, 2004 | Sheet 17 of 58


32K suspend clock output
SB400 SB
Part 1 of 4
MAIN SOURCE: 82.30001.031 EPSON
2ND SOURCE: 82.30001.341 KDS
PCIRST# 3V to 5V level shift for HDD & CDROM
SB400 asserts PLTRST# to reset devices on the platform.
Secondary PCI Bus reset signal.
Pull up 100k to 3D3V_S0
?which is gnd
CHS-215SB400
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ATI-SB400 (1 of 5) PCI, PCIE
Size A3
Document Number
Bolsena
Rev SA
Date: Tuesday, December 28, 2004
Sheet 18 of 58





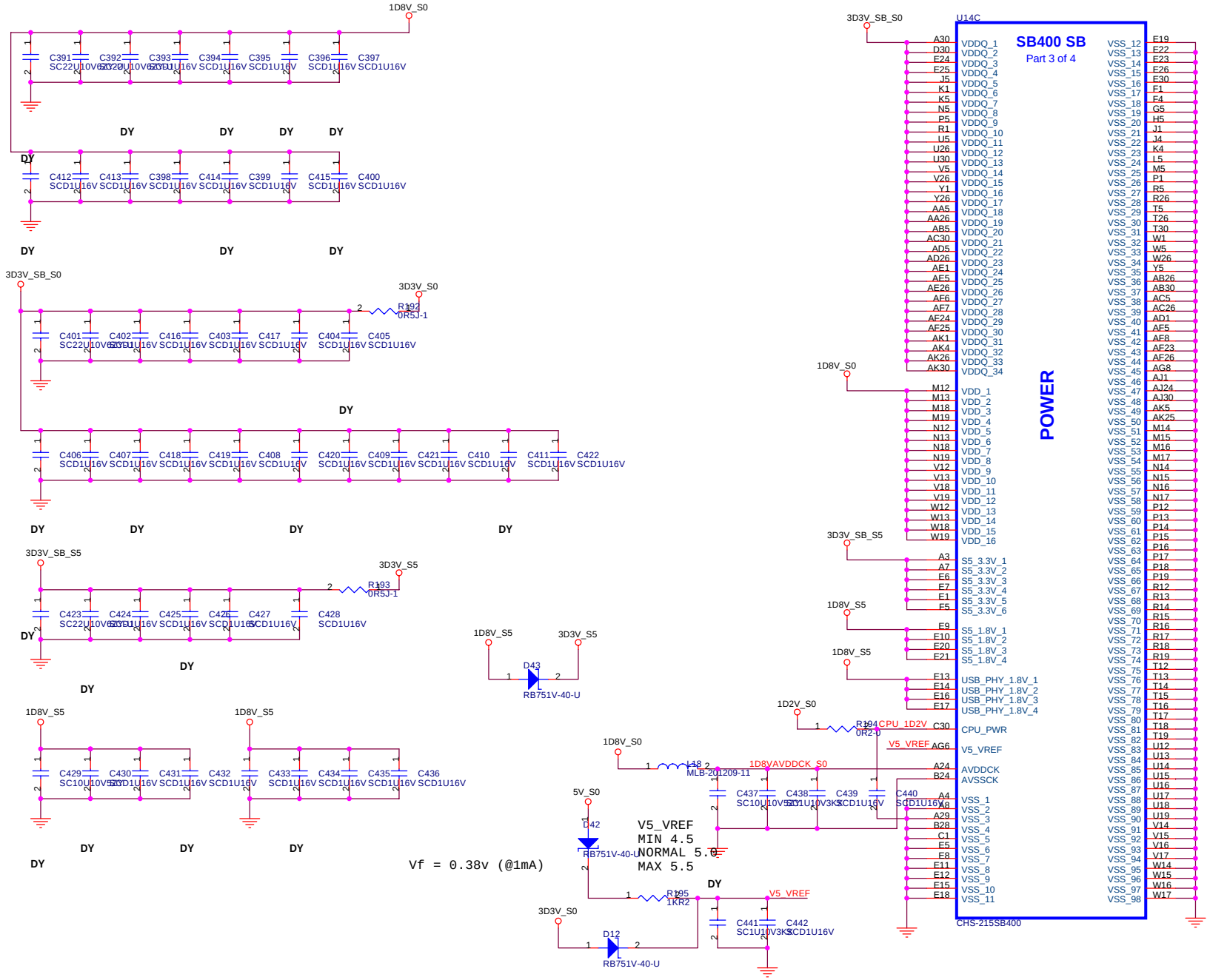
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATI-SB400 (2 of 5) IDE**

Size: A3 | Document Number: **Bolsena** | Rev: SA

Date: Tuesday, December 28, 2004 | Sheet 19 of 58



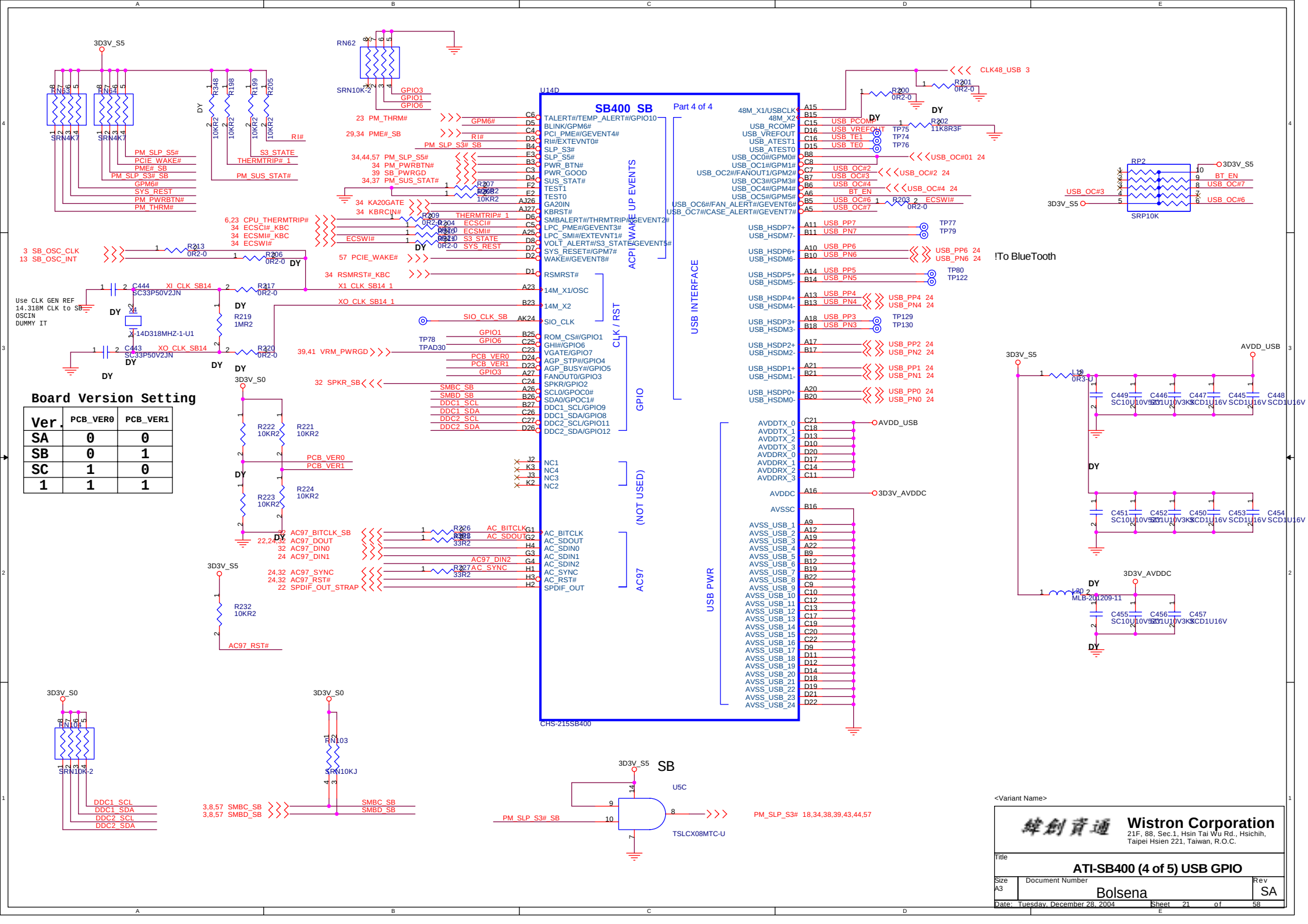
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI-SB400 (3 of 5) POWER

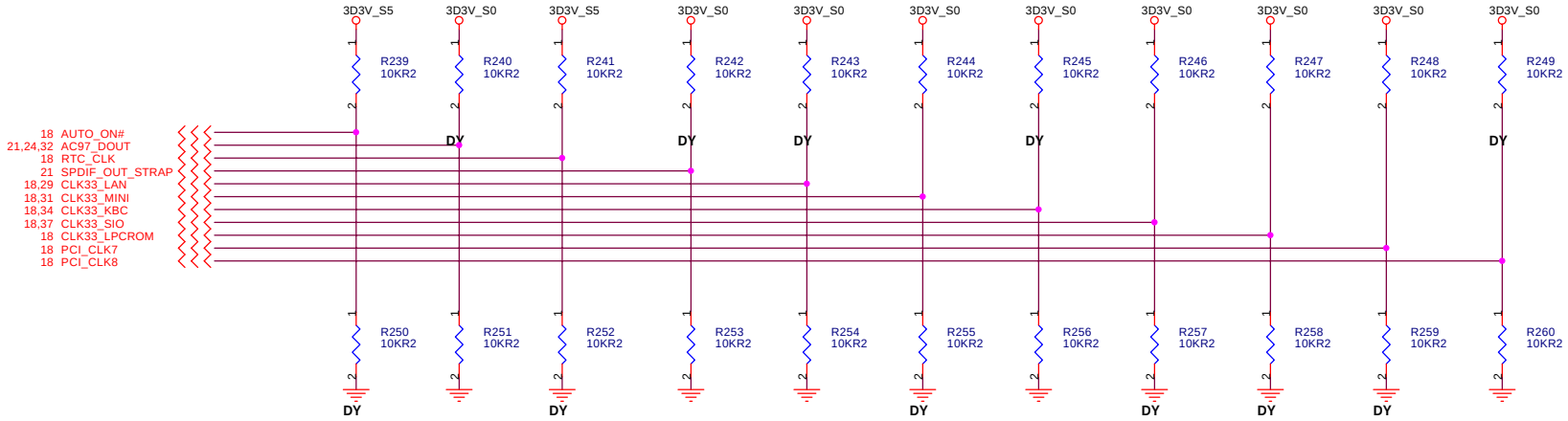
Size	Document Number	Rev
A3	Bolsena	SA

Date: Tuesday, December 28, 2004 Sheet 20 of 58



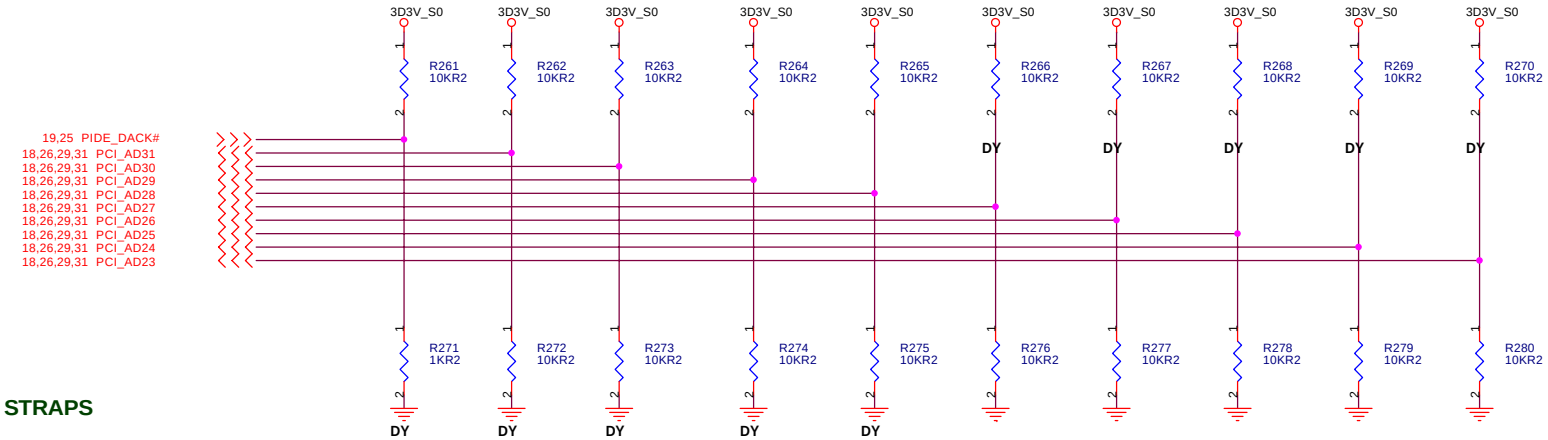
Board Version Setting

Ver.	PCB_VER0	PCB_VER1
SA	0	0
SB	0	1
SC	1	0
1	1	1



REQUIRED SYSTEM STRAPS

	ACPWRON	AC_SDOUT	RTC_CLK	SPDIF_OUT	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	PCI_CLK6	PCI_CLK7 PCI_CLK8
STRAP HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	SIO 24MHz	48MHZ-Clock Input Buffer DEFAULT	USB PHY PWRDOWN DISABLE DEFAULT	USB INT PLL48 DEFAULT	14MHZ OSC MODE DEFAULT	CPU I/F=K8 DEFAULT	ROM TYPE H,H=PCI (X Bus) ROM H,L=LPC ROM I
STRAP LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTENNAL RTC (NOT SUPPORTED W/IT8712)	SIO 48MHz DEFAULT	48MHZ -Crytsal Pad	USB PHY PWRDOWN ENABLE	USB EXT. 48MHZ	14MHZ XTAL MODE	CPU I/F=P4	L,H=LPC ROM II L,L=Firmware Hub ROM



DEBUG STRAPS

	PDACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
STRAP HIGH	USE LONG RESET DEFAULT	RESERVED	RESERVED	RESERVED	RESERVED	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	RESERVED
STRAP LOW	USE SHORT RESET					USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	

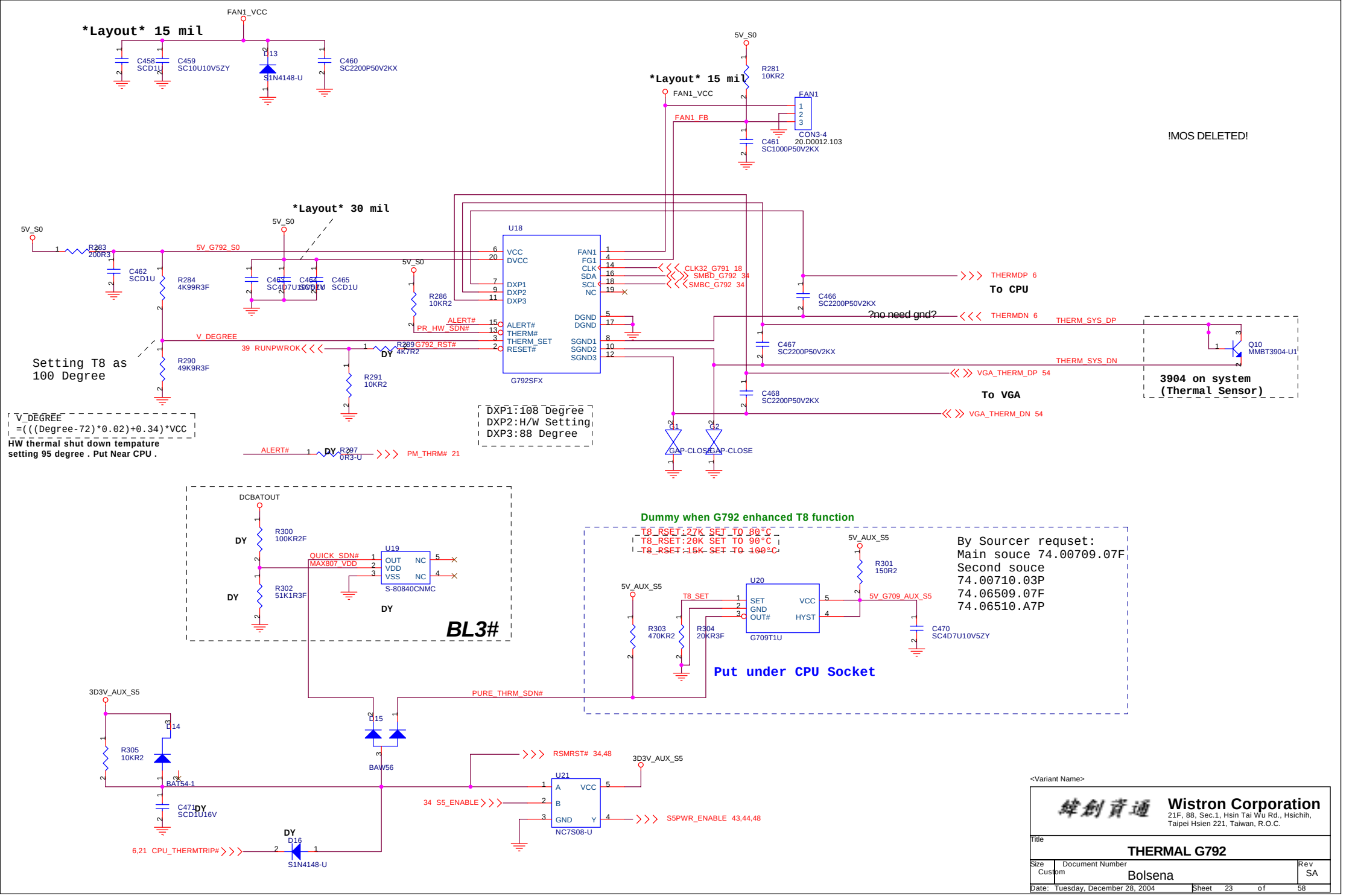
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI-SB400 STRAPPING(5 of 5)

Size: A3 | Document Number: Bolsena | Rev: SA

Date: Tuesday, December 28, 2004 | Sheet 22 of 58



<Variant Name>

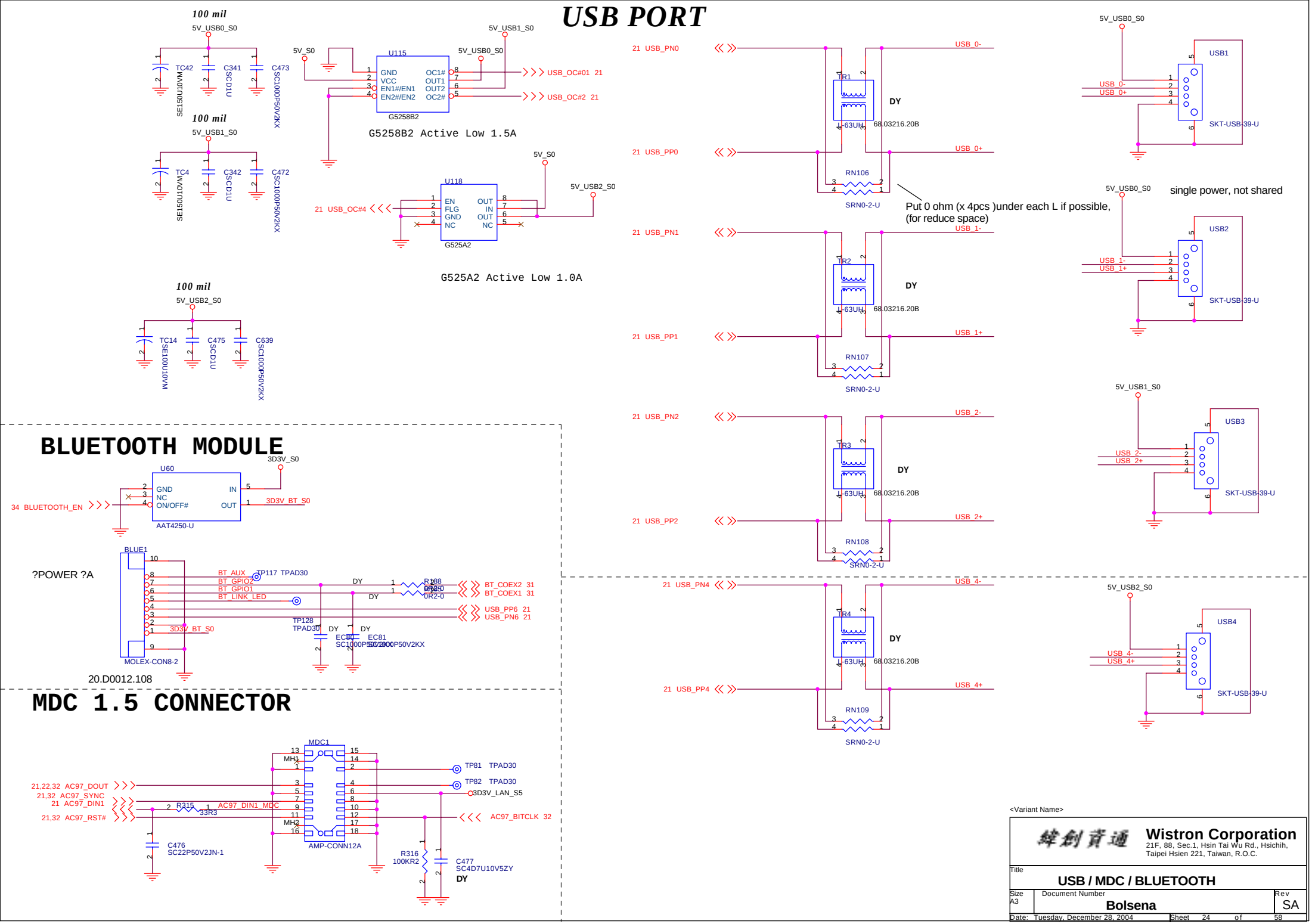
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **THERMAL G792**

Size	Document Number	Rev
Custom	Bolsena	SA

Date: Tuesday, December 28, 2004 Sheet 23 of 58

USB PORT



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

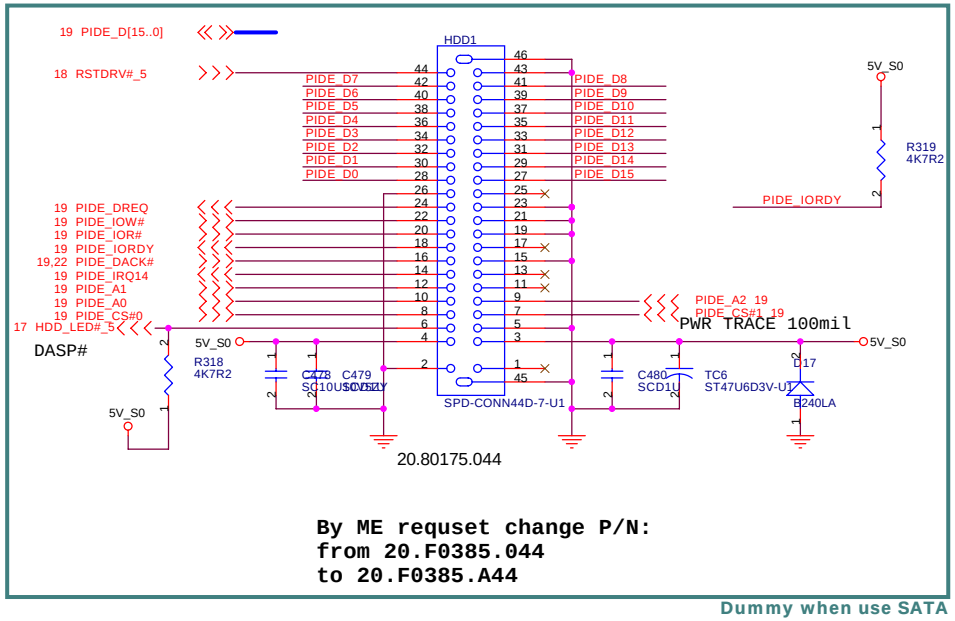
Title: **USB / MDC / BLUETOOTH**

Size	Document Number	Rev
A3	**Bolsena**	SA

Date: Tuesday, December 28, 2004 Sheet 24 of 58

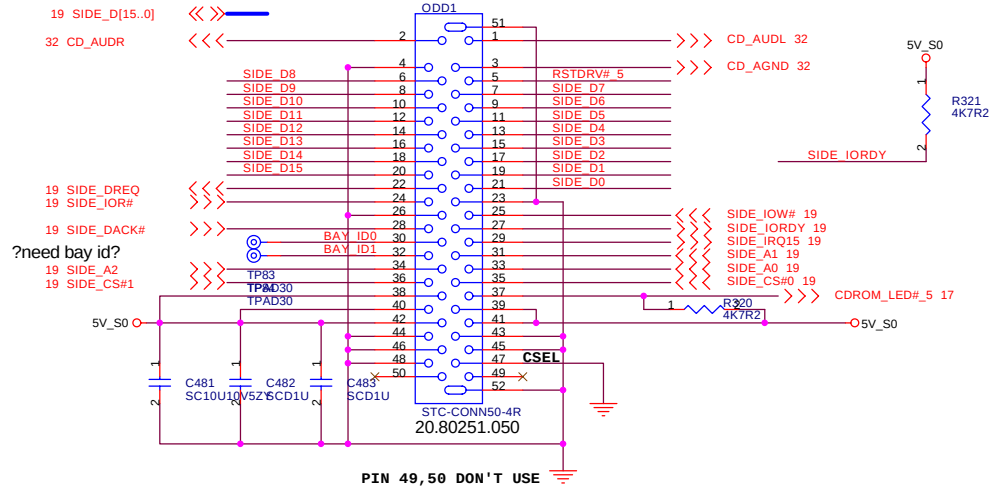
HDD

?direction ok?

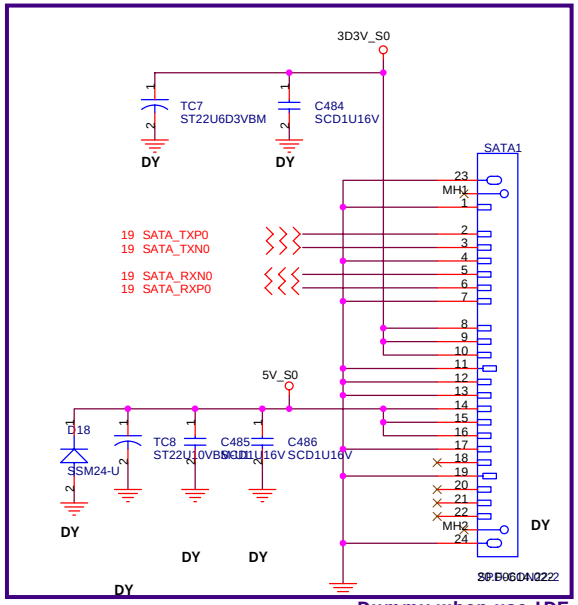


Dummy when use SATA

CDROM



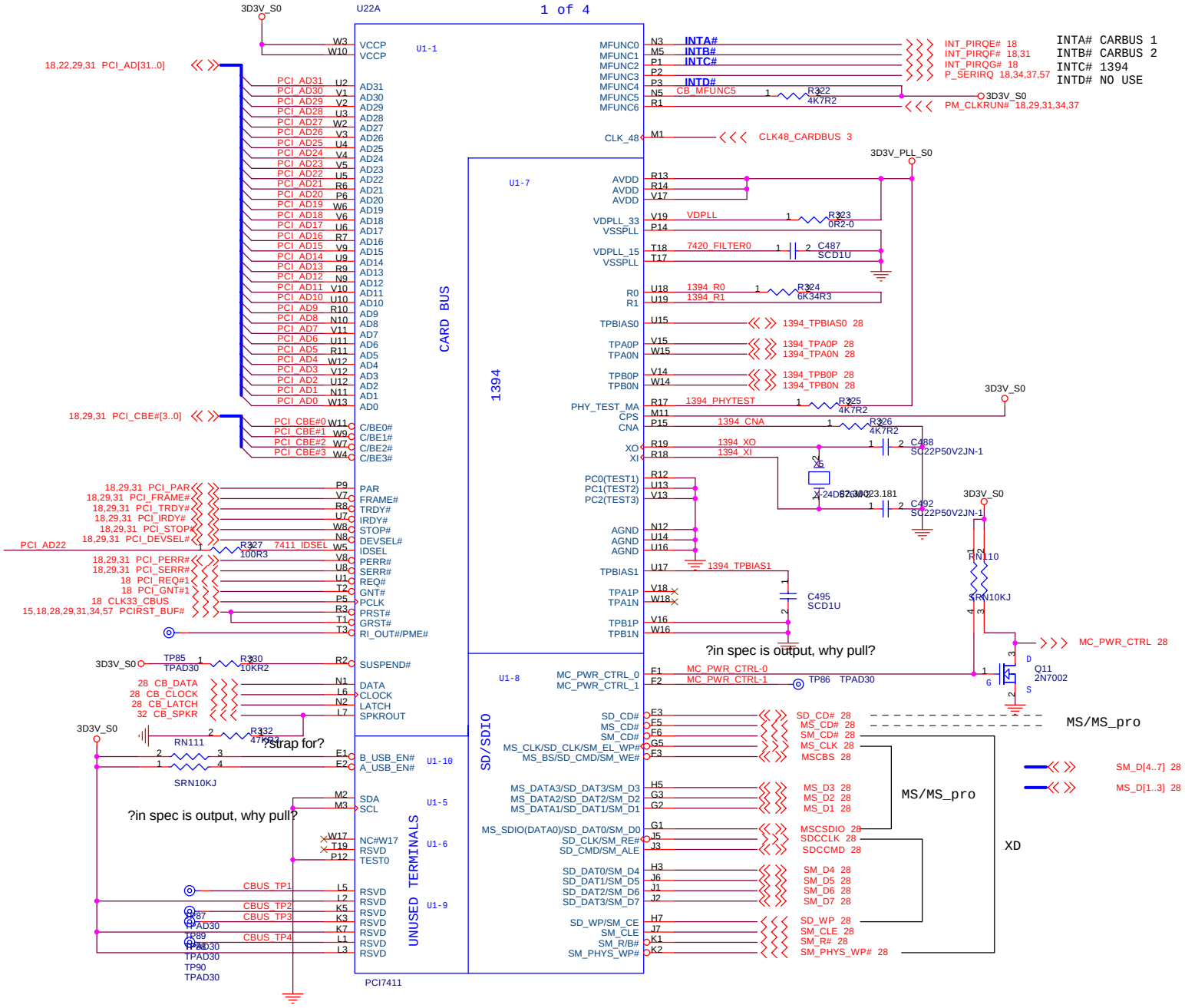
SATA Connector



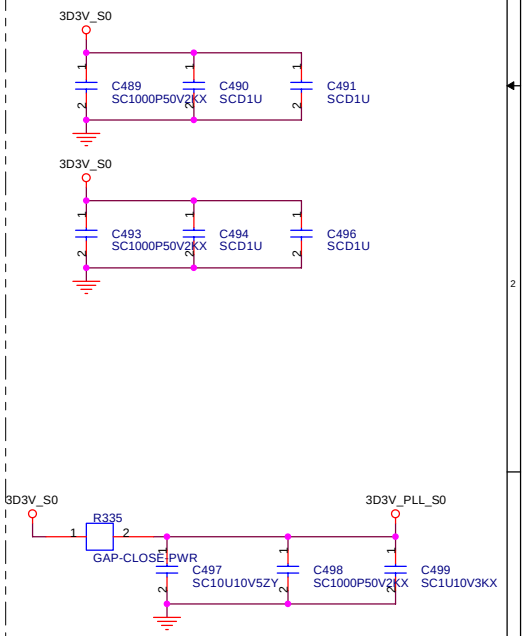
Dummy when use IDE

<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**HDD / CDROM / SATA**	
Size A3	Document Number **Bolsena**	Rev SA
Date: Tuesday, December 28, 2004	Sheet 25 of 58	



Bypass/Decupoling Capacitors
Should be places as close to
PCI7411 as possible



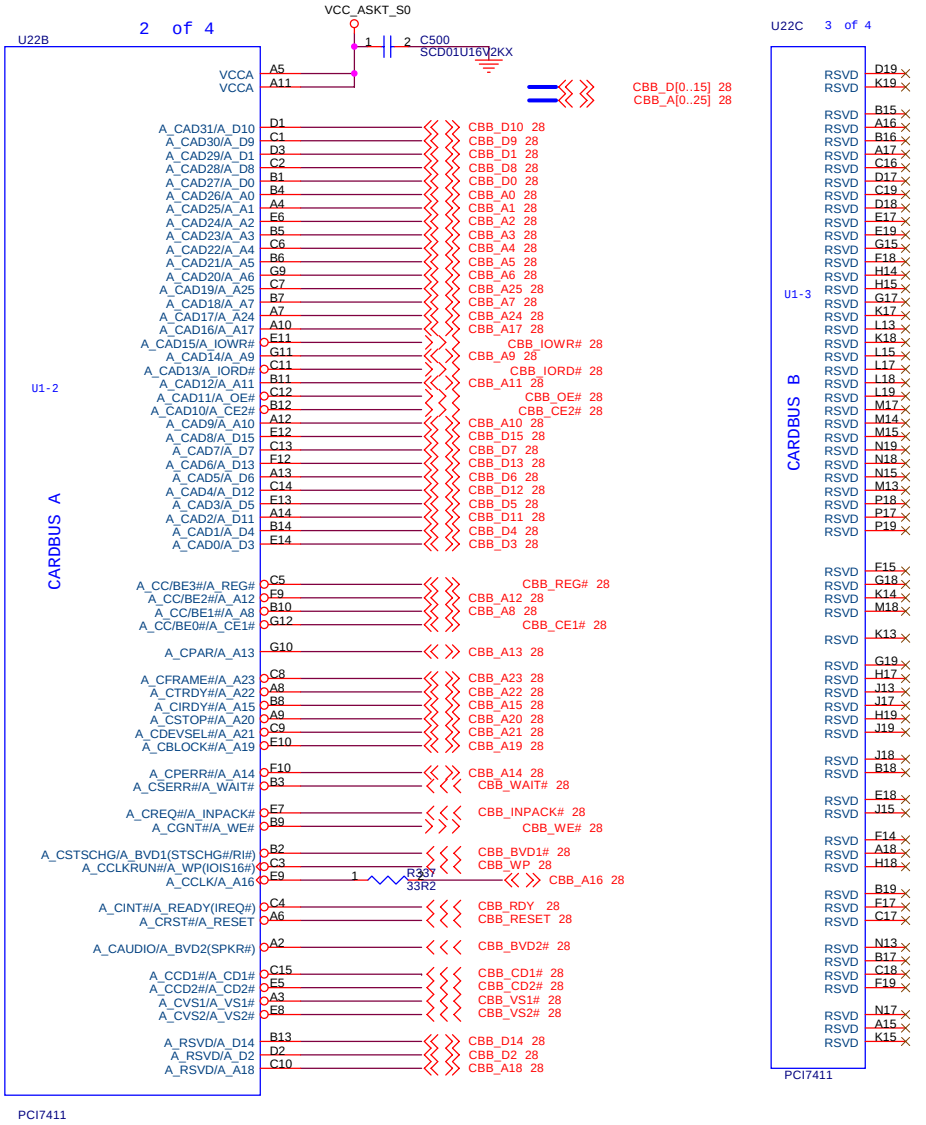
<Variant Name>

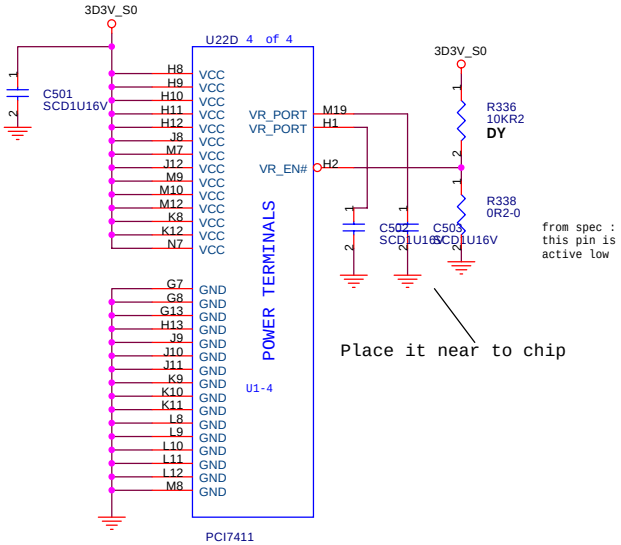
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **TI_PCI7411(1 of 2)**

Size: A3 | Document Number: **Bolsena** | Rev: SA

Date: Tuesday, December 28, 2004 | Sheet 26 of 58





<Variant Name>

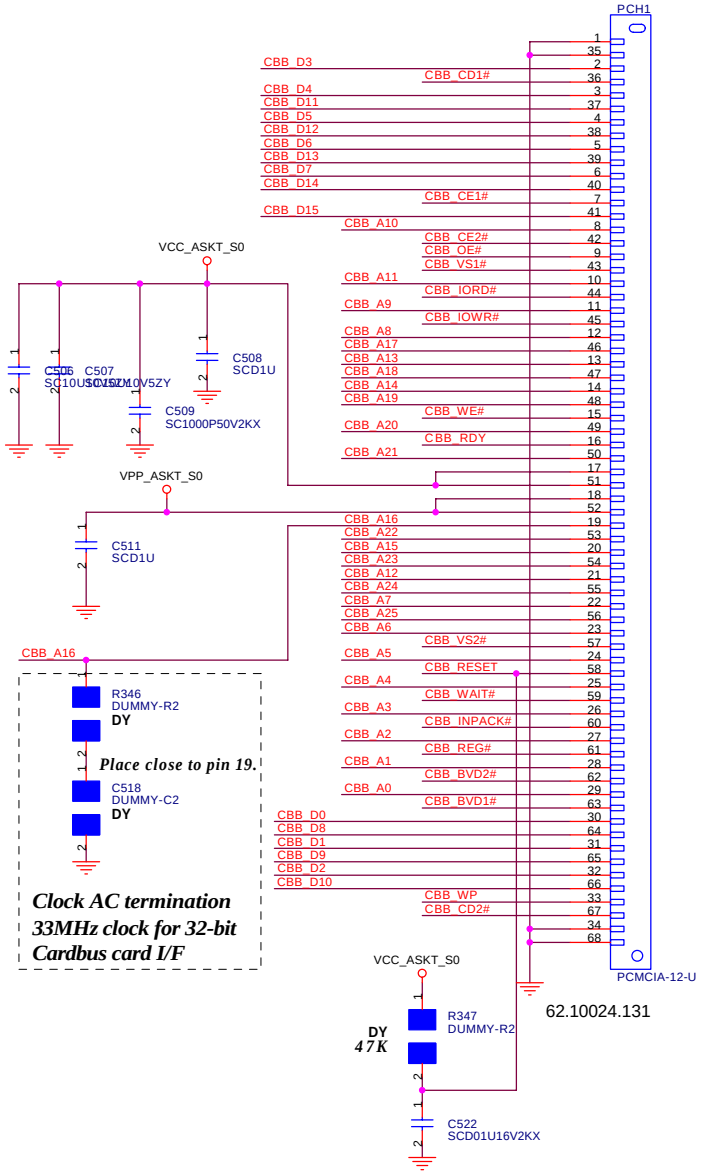
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **TI_PCI7411(2 of 2)**

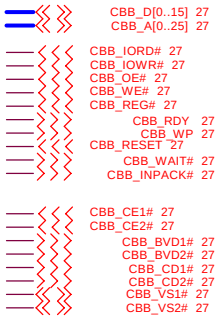
Size: A3 | Document Number: **Bolsena** | Rev: SA

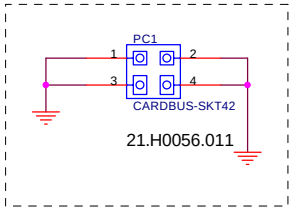
Date: Tuesday, December 28, 2004 | Sheet 27 of 58

PCMCIA Socket

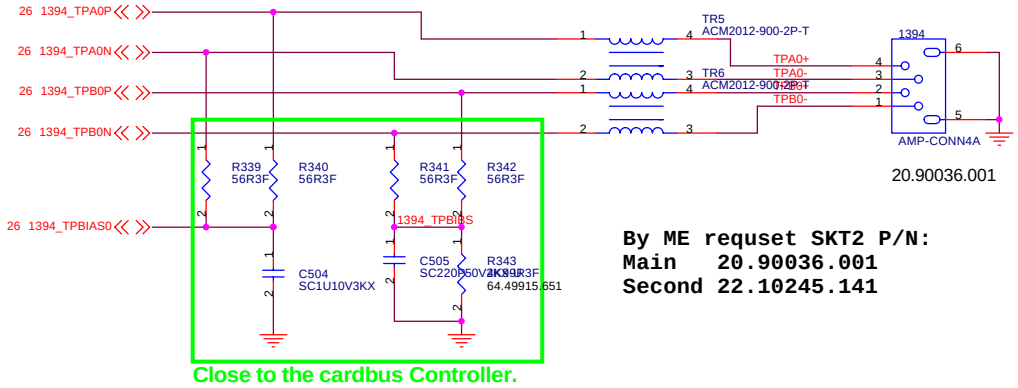


Cardbus I/F



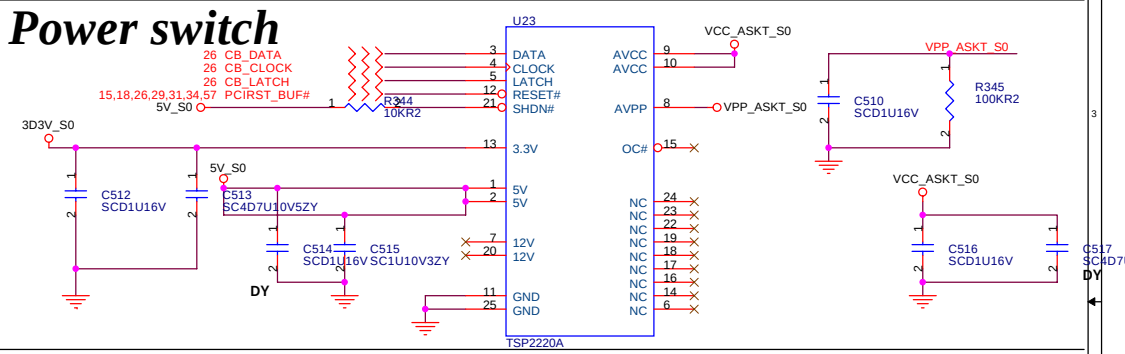


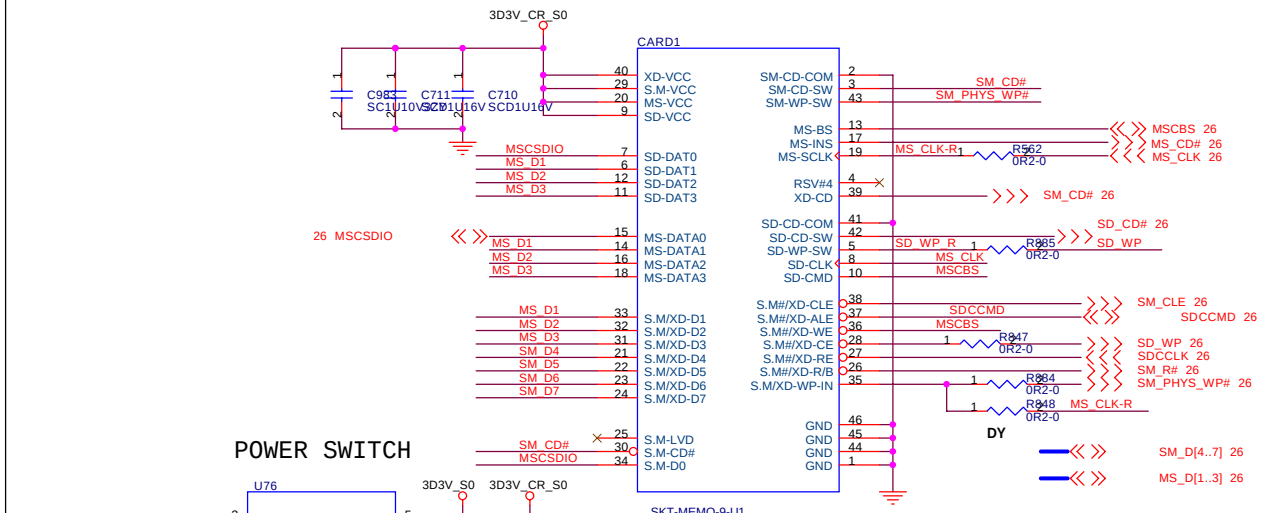
1394 Connector



By ME requset SKT2 P/N:
Main 20.90036.001
Second 22.10245.141

Power switch





<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCMCA / 1394 / CARD READER

Size: A3 | Document Number: Bolsena | Rev: SA

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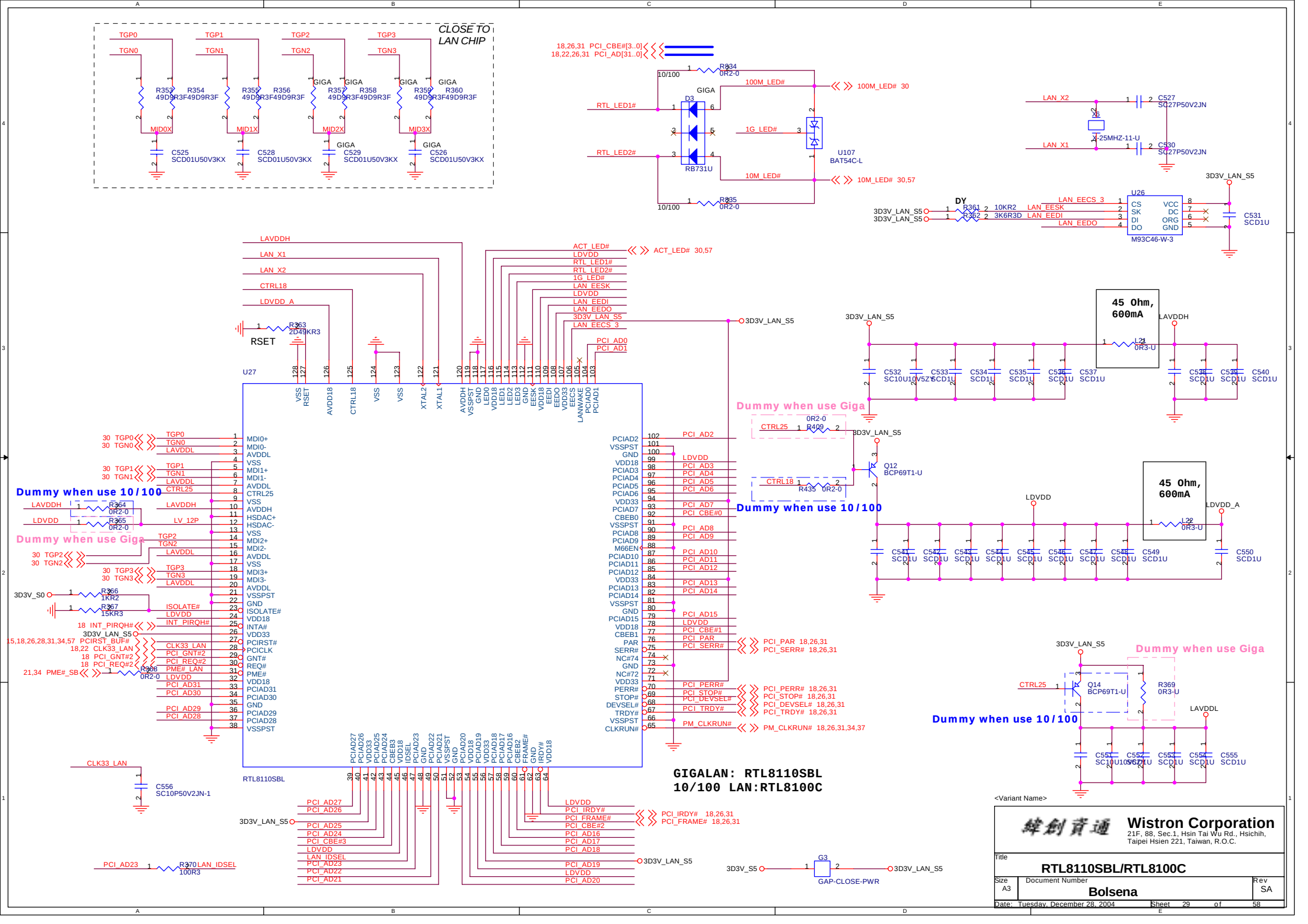
CLOSE TO LAN CHIP
TGP0
TGN0
TGP1
TGN1
TGP2
TGN2
TGP3
TGN3
R352 49D9R3F
R354 49D9R3F
R355 49D9R3F
R356 49D9R3F
R357 49D9R3F
R358 49D9R3F
R359 49D9R3F
R360 49D9R3F
GIGA
MID0X
MID1X
MID2X
MID3X
C525 SCD01U50V3KX
C528 SCD01U50V3KX
C529 SCD01U50V3KX
C526 SCD01U50V3KX
18,26,31 PCI_CBE#[3..0]
18,22,26,31 PCI_AD[31..0]
R334 0R2-0
10/100
RTL_LED1#
RTL_LED2#
D3
RB731U
100M_LED#
1G_LED#
10M_LED#
100M_LED# 30
10M_LED# 30,57
U107 BAT54C-L
R335 0R2-0
LAN_X2
LAN_X1
C527 SC27P50V2JN
C530 SC27P50V2JN
X-25MHZ-11-U
3D3V_LAN_S5
DY
R361 10KR2
R362 3K6R3D
LAN_EECS_3
LAN_EESK
LAN_EEDI
LAN_EEDO
U26
CS
SK
DI
DO
VCC
DC
ORG
GND
M93C46-W-3
C531 SCD1U
LAVDDH
LAN_X1
LAN_X2
CTRL18
LDVDD_A
R363 2D49KR3
RSET
ACT_LED#
LDVDD
RTL_LED1#
RTL_LED2#
1G_LED#
LAN_EESK
LAN_EEDI
LAN_EEDO
3D3V_LAN_S5
LAN_EECS_3
PCI_AD0
PCI_AD1
ACT_LED# 30,57
U27
VSS
RSET
AVDD18
CTRL18
XTAL2
XTAL1
VSSPST
GND
LED0
VDD18
LED1
LED2
LED3
EESK
EEDI
EEDO
VDD33
EECS
LANWAKE
PCIAD0
PCIAD1
MDI0+
MDI0-
AVDDL
MDI1+
MDI1-
CTRL25
AVDDH
HSDAC+
HSDAC-
MDI2+
MDI2-
MDI3+
MDI3-
INITA#
VDD33
PCIRST#
PCICLK
GNT#
REQ#
PME#
PCIAD31
PCIAD30
PCIAD29
PCIAD28
PCIAD2
PCIAD3
PCIAD4
PCIAD5
PCIAD6
M66EN
PCIAD10
PCIAD11
PCIAD12
PCIAD13
PCIAD14
PCIAD15
CBEB1
PAR
SERR#
NC#74
NC#72
PERR#
STOP#
DEVSEL#
TRDY#
CLKRUN#
PCIAD27
PCIAD26
PCIAD25
PCIAD24
CBEB3
IDSEL
PCIAD23
PCIAD22
PCIAD21
PCIAD20
PCIAD19
PCIAD18
PCIAD17
PCIAD16
CBEB2
FRAME#
IRDY#
RTL8110SBL
30 TGP0
30 TGN0
30 TGP1
30 TGN1
30 TGP2
30 TGN2
30 TGP3
30 TGN3
LV_12P
Dummy when use 10/100
Dummy when use Giga
R364 0R2-0
R365 0R2-0
3D3V_S0
R366 1KR2
R367 15KR3
ISOLATE#
INT_PIRQH#
18 INT_PIRQH#
15,18,26,28,31,34,57 PCIRST_BUF#
18,22 CLK33_LAN
18 PCI_GNT#2
18 PCI_REQ#2
21,34 PME#_SB
R368 0R2-0
PCI_AD31
PCI_AD30
PCI_AD29
PCI_AD28
PCI_AD2
PCI_AD3
PCI_AD4
PCI_AD5
PCI_AD6
PCI_AD7
PCI_CBE#0
PCI_AD8
PCI_AD9
PCI_AD10
PCI_AD11
PCI_AD12
PCI_AD13
PCI_AD14
PCI_AD15
PCI_CBE#1
PCI_PAR
PCI_SERR#
PCI_PAR 18,26,31
PCI_SERR# 18,26,31
PCI_PERR#
PCI_STOP#
PCI_DEVSEL#
PCI_TRDY#
PCI_PERR# 18,26,31
PCI_STOP# 18,26,31
PCI_DEVSEL# 18,26,31
PCI_TRDY# 18,26,31
PM_CLKRUN#
PM_CLKRUN# 18,26,31,34,37
CTRL25
R409 0R2-0
CTRL18
R435 0R2-0
Q12 BCP69T1-U
45 Ohm, 600mA
L21 0R3-U
L22 0R3-U
LDVDD
LAVDDL
C532 SC10U10V5ZY
C533 SCD1U
C534 SCD1U
C535 SCD1U
C536 SCD1U
C537 SCD1U
C538 SCD1U
C539 SCD1U
C540 SCD1U
C541 SCD1U
C542 SCD1U
C543 SCD1U
C544 SCD1U
C545 SCD1U
C546 SCD1U
C547 SCD1U
C548 SCD1U
C549 SCD1U
C550 SCD1U
Q14 BCP69T1-U
R369 0R3-U
C551 SC10U10V5ZY
C552 SCD1U
C553 SCD1U
C554 SCD1U
C555 SCD1U
CLK33_LAN
C556 SC10P50V2JN-1
PCI_AD27
PCI_AD26
PCI_AD25
PCI_AD24
PCI_CBE#3
LDVDD
LAN_IDSEL
PCI_AD23
PCI_AD22
PCI_AD21
PCI_IRDY#
PCI_FRAME#
PCI_CBE#2
PCI_AD16
PCI_AD17
PCI_AD18
PCI_AD19
PCI_AD20
PCI_IRDY# 18,26,31
PCI_FRAME# 18,26,31
R370 100R3
3D3V_S5
G3
GAP-CLOSE-PWR
GIGALAN: RTL8110SBL
10/100 LAN:RTL8100C
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
RTL8110SBL/RTL8100C
Size A3
Document Number
Bolsena
Rev SA
Date: Tuesday, December 28, 2004
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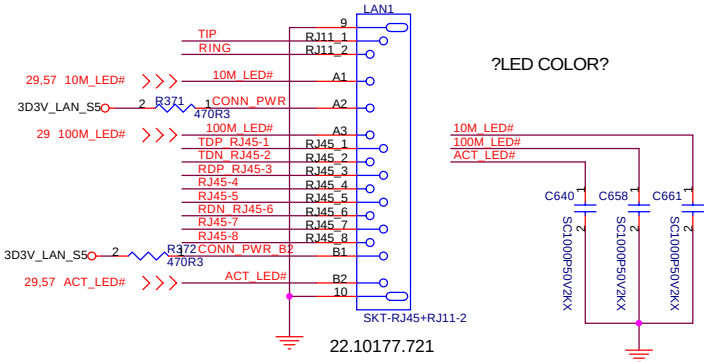
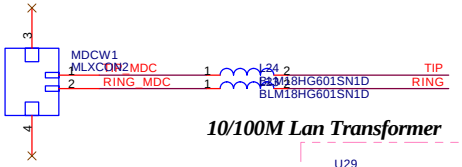
Link: Green - 10Mbps/802.11b
Orange - 100Mbps/802.11a
Yellow - 1Gbps

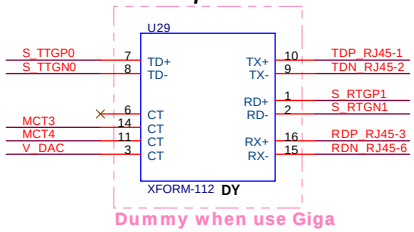
Activity: Yellow



?LED COLOR?



10/100M Lan Transformer



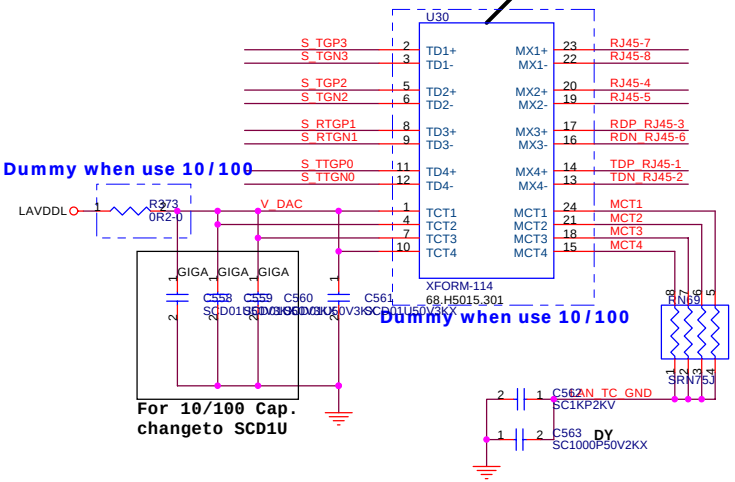
Dummy when use Giga

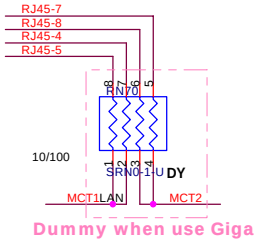
By Sourcer requset change P/N:
From 68.H0013.301
To 68.0H80P.301

By Sourcer requset change P/N:
From 68.H5015.301
To 68.02402.30A

GIGA Lan Transformer

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

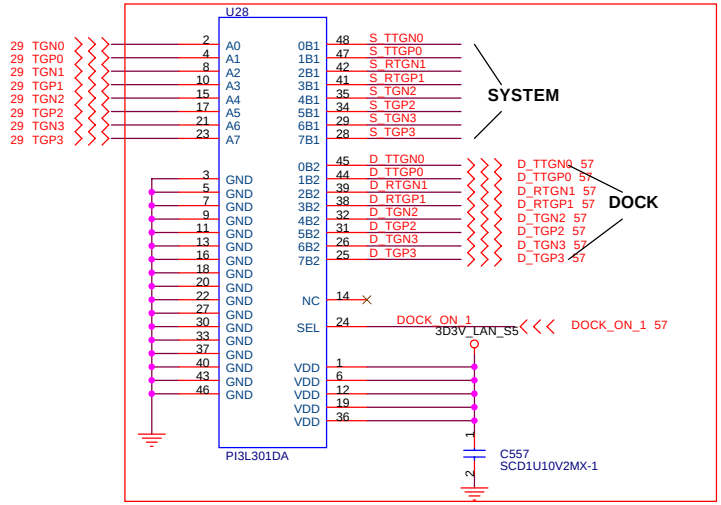




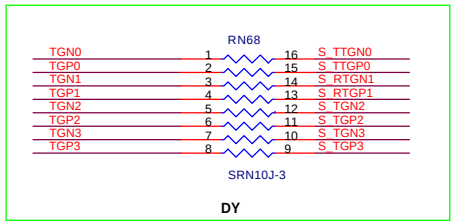
Dummy when use Giga

Function	SEL
An to nB1	L
An to nB2	H

LAN switch



Dummy when no EZ4



Dummy when use EZ4

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN CONN

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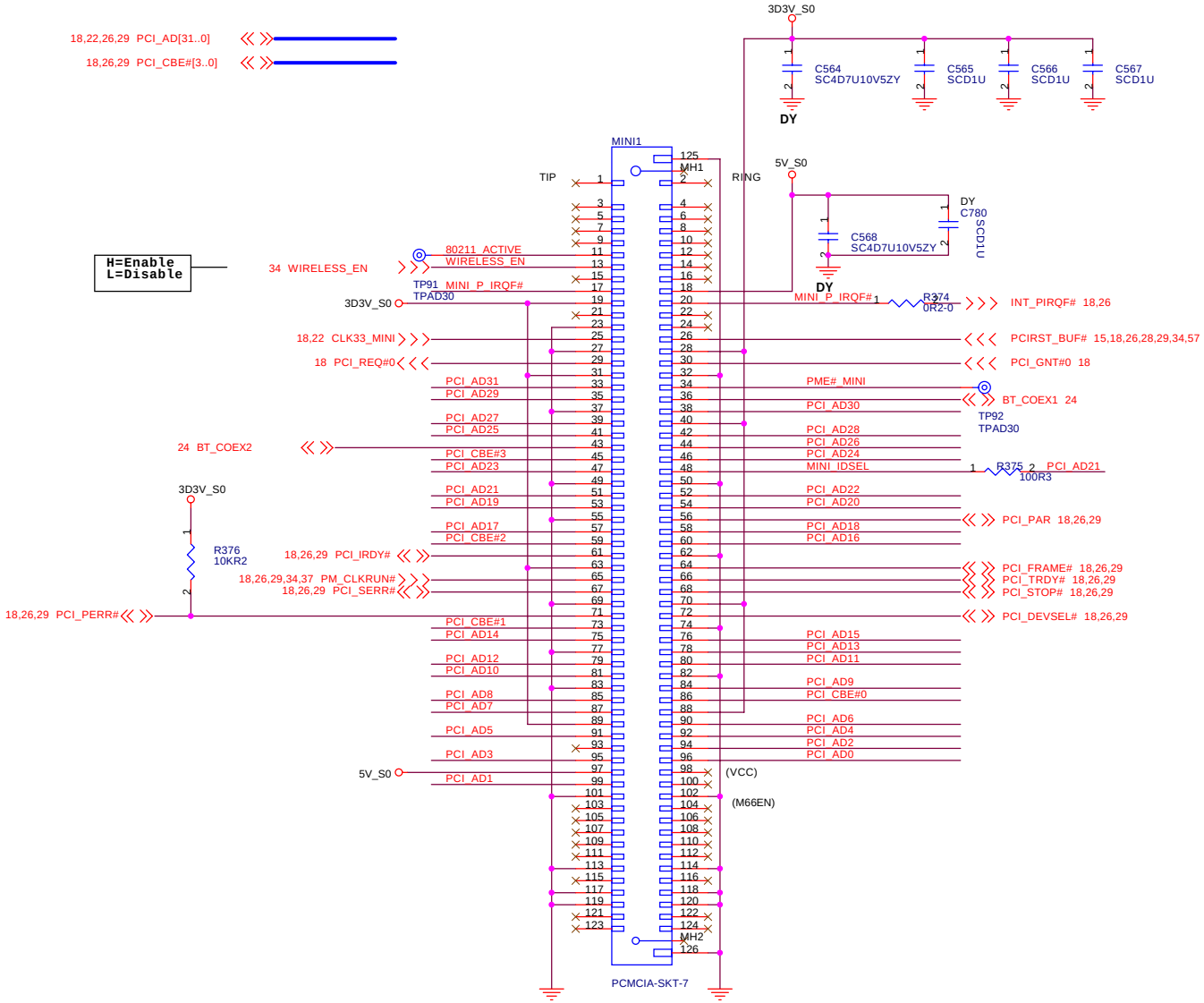
MINI-PCI



62.10071.001

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **MINI-PCI**

Size: A3 | Document Number: **Bolsena** | Rev: SA

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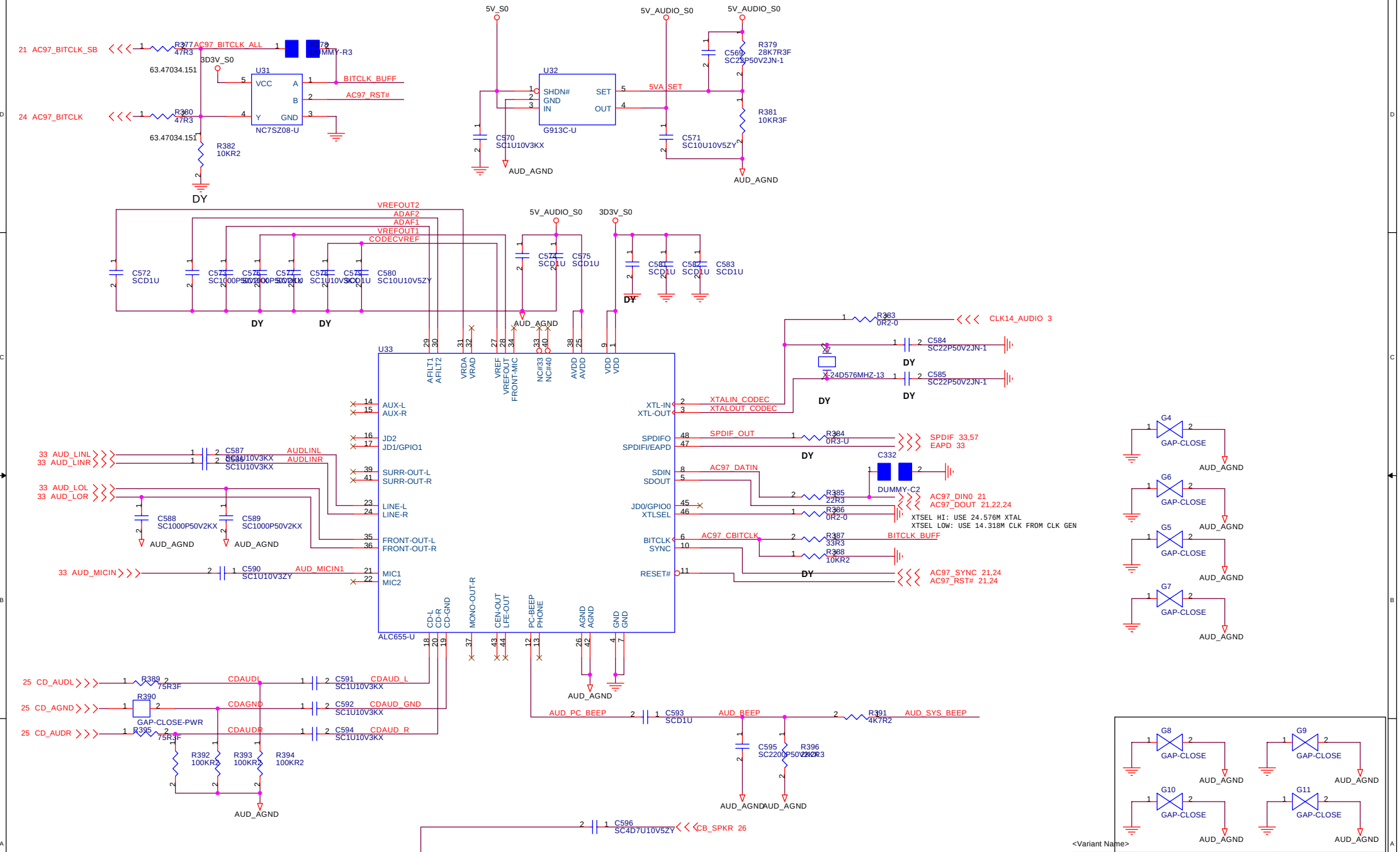

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO (1/2) -- CODEC ALC655

Size: A3 | Document Number: Bolsena | Rev: SA

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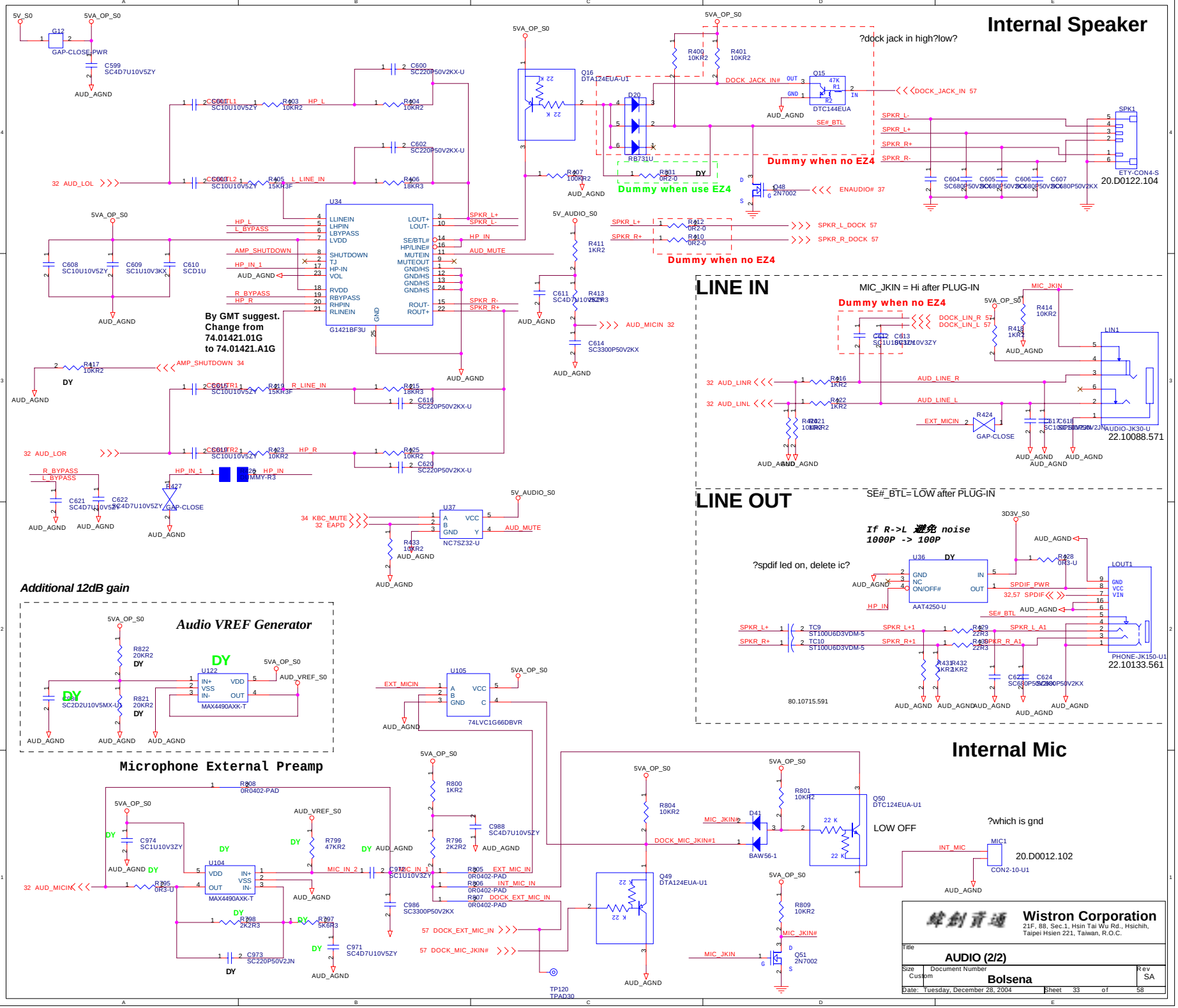
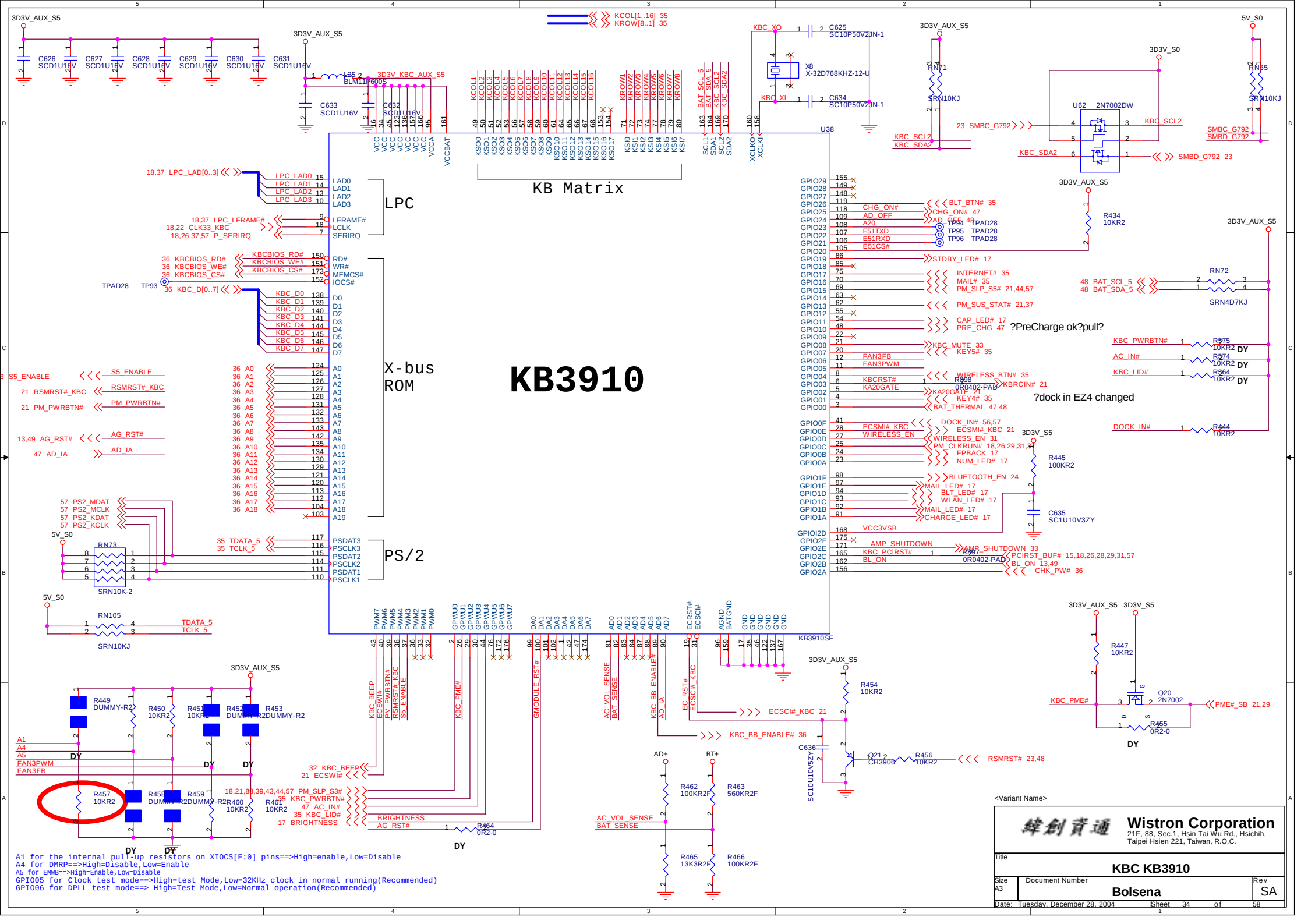
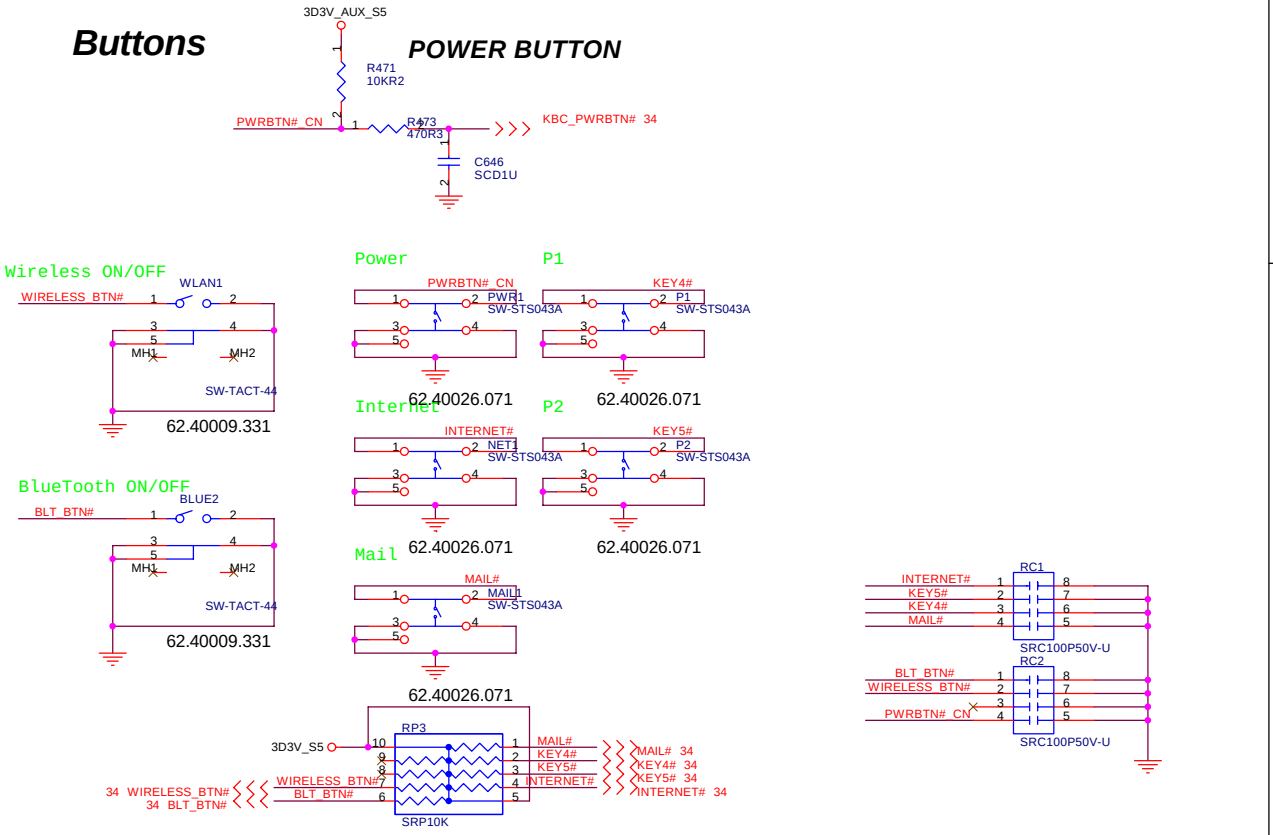
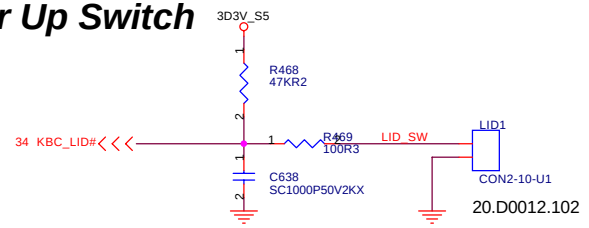

Internal Speaker
?dock jack in high?low?
Dummy when no EZ4
Dummy when use EZ4
Dummy when no EZ4
SPK1
ETY-CON4-S
20.D0122.104
U34
G1421BF3U
By GMT suggest.
Change from
74.01421.01G
to 74.01421.A1G
LINE IN
MIC_JKIN = Hi after PLUG-IN
Dummy when no EZ4
LIN1
AUDIO-JK30-U
22.10088.571
LINE OUT
SE#_BTL= LOW after PLUG-IN
If R->L 避免 noise
1000P -> 100P
?spdif led on, delete ic?
U36
AAT4250-U
LOUT1
PHONE-JK150-U1
22.10133.561
80.10715.591
Additional 12dB gain
Audio VREF Generator
U122
MAX4490AXK-T
Microphone External Preamp
U104
MAX4490AXK-T
U105
74LVC1G66DBVR
U37
NC7SZ32-U
Internal Mic
?which is gnd
MIC1
CON2-10-U1
20.D0012.102
LOW OFF
Q50
DTC124EUA-U1
Q49
DTA124EUA-U1
Q51
2N7002
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
AUDIO (2/2)
Size Custom
Document Number
Bolsena
Rev SA
Date: Tuesday, December 28, 2004
Sheet 33 of 58


KB3910
KB Matrix
LPC
X-bus ROM
PS/2
U38
KB3910SF
3D3V_AUX_S5
3D3V_S0
5V_S0
3D3V_S5
KCOL[1..16] 35
KROW[8..1] 35
KBC_XO
KBC_XI
X8 X-32D768KHZ-12-U
C625 SC10P50V2JN-1
C634 SC10P50V2JN-1
U62 2N7002DW
KBC_SCL2
KBC_SDA2
SMBC_G792
SMBD_G792
LPC_LAD[0..3]
LPC_LFRAME#
CLK33_KBC
P_SERIRQ
KBCBIOS_RD#
KBCBIOS_WE#
KBCBIOS_CS#
KBC_D[0..7]
TPAD28
TP93
S5_ENABLE
RSMRST#_KBC
PM_PWRBTN#
AG_RST#
AD_IA
PS2_MDAT
PS2_MCLK
PS2_KDAT
PS2_KCLK
TDATA_5
TCLK_5
RN73
SRN10K-2
RN105
SRN10KJ
RN71
RN65
RN72
SRN4D7KJ
R434 10KR2
R445 100KR2
C635 SC1U10V3ZY
R447 10KR2
Q20 2N7002
R455 0R2-0
R454 10KR2
Q21 CH3906
R456 10KR2
C636 SC10U10V5ZY
R462 100KR2F
R463 560KR2F
R465 13K3R2F
R466 100KR2F
R464 0R2-0
R449 DUMMY-R2
R450 10KR2
R451 10KR2
R452 DUMMY-R2
R453 DUMMY-R2
R457 10KR2
R458 DUMMY-R2
R459 DUMMY-R2
R460 10KR2
R461 10KR2
DY
KBC_BEEP
ECSWI#
PM_PWRBTN#
RSMRST#_KBC
S5_ENABLE
KBC_PME#
GMODULE_RST#
AC_VOL_SENSE
BAT_SENSE
KBC_BB_ENABLE#
AD_IA
EC_RST#
ECSCI#_KBC
BRIGHTNESS
AG_RST#
PM_SLP_S3#
KBC_PWRBTN#
AC_IN#
KBC_LID#
ECSCI#_KBC 21
KBC_BB_ENABLE# 36
RSMRST# 23,48
PME#_SB 21,29
BLT_BTN# 35
CHG_ON# 47
AD_OFF 48
STDBY_LED# 17
INTERNET# 35
MAIL# 35
PM_SLP_SS# 21,44,57
PM_SUS_STAT# 21,37
CAP_LED# 17
PRE_CHG 47
?PreCharge ok?pull?
KBC_MUTE 33
KEY5# 35
WIRELESS_BTN# 35
KBRCIN# 21
KEY4# 35
BAT_THERMAL 47,48
DOCK_IN# 56,57
ECSMI#_KBC 21
WIRELESS_EN 31
PM_CLKRUN# 18,26,29,31,47
FPBACK 17
NUM_LED# 17
?dock in EZ4 changed
BLUETOOTH_EN 24
MAIL_LED# 17
BLT_LED# 17
WLAN_LED# 17
CHARGE_LED# 17
AMP_SHUTDOWN 33
PCIRST_BUF# 15,18,26,28,29,31,57
BL_ON 13,49
CHK_PW# 36
A1 for the internal pull-up resistors on XIOCS[F:0] pins==>High=enable,Low=Disable
A4 for DMRP==>High=Disable,Low=Enable
A5 for EMWB==>High=Enable,Low=Disable
GPIO05 for Clock test mode==>High=test Mode,Low=32KHz clock in normal running(Recommended)
GPIO06 for DPLL test mode==> High=Test Mode,Low=Normal operation(Recommended)
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
KBC KB3910
Size A3
Document Number
Bolsena
Rev SA
Date: Tuesday, December 28, 2004
Sheet 34 of 58

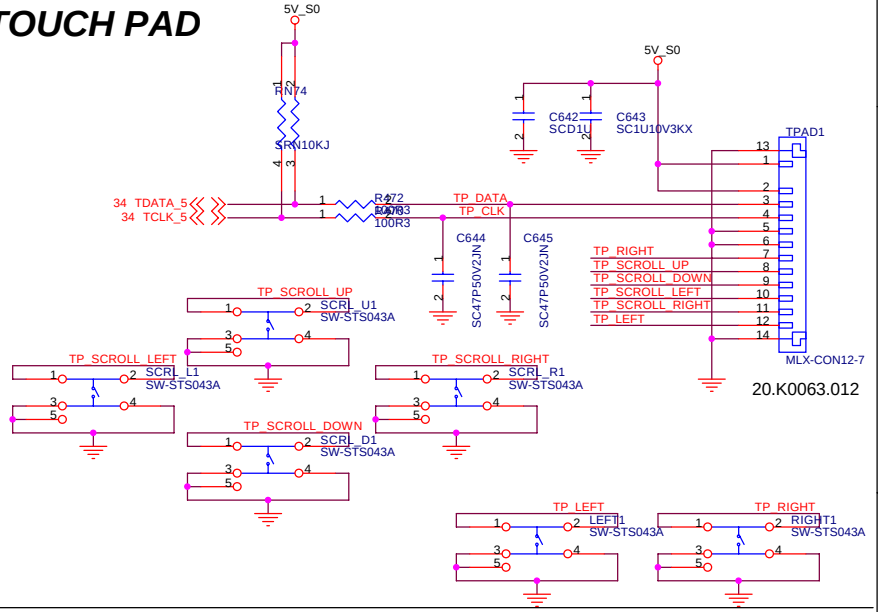
Buttons



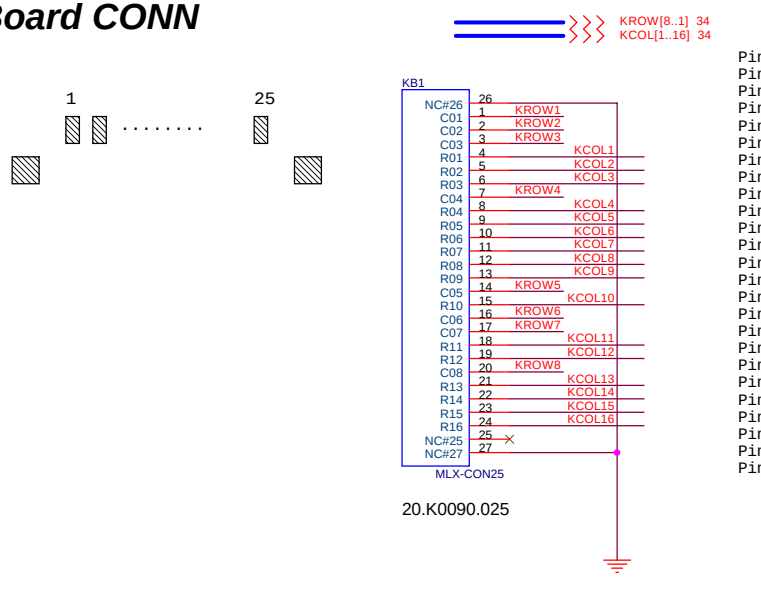
Cover Up Switch



TOUCH PAD

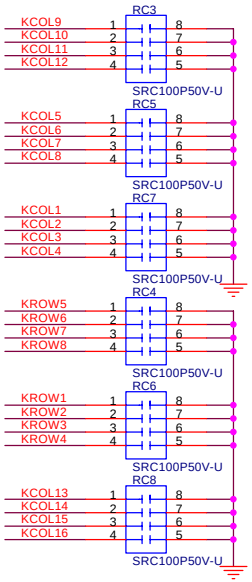


Internal KeyBoard CONN



Pin1 ==>*R01
Pin2 ==>*R02
Pin3 ==>*R03
Pin4 ==> C01
Pin5 ==> C02
Pin6 ==> C03
Pin7 ==>*R04
Pin8 ==> C04
Pin9 ==> C05
Pin10 ==> C06
Pin11 ==> C07
Pin12 ==> C08
Pin13 ==> C09
Pin14 ==>*R05
Pin15 ==> C10
Pin16 ==>*R06
Pin17 ==>*R07
Pin18 ==> C11
Pin19 ==> C12
Pin20 ==>*R08
Pin21 ==> C13
Pin22 ==> C14
Pin23 ==> C15
Pin24 ==> C16
Pin25 ==> NC

EMI Bypass cap.



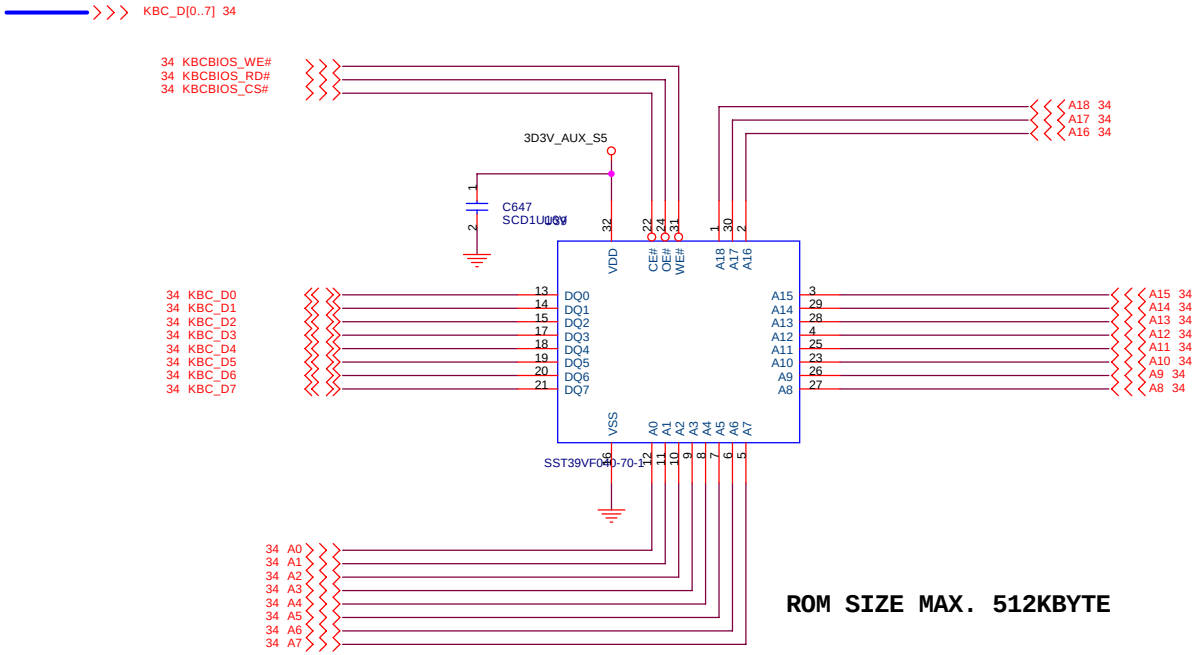
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BUTTONs / KB / TOUCHPAD

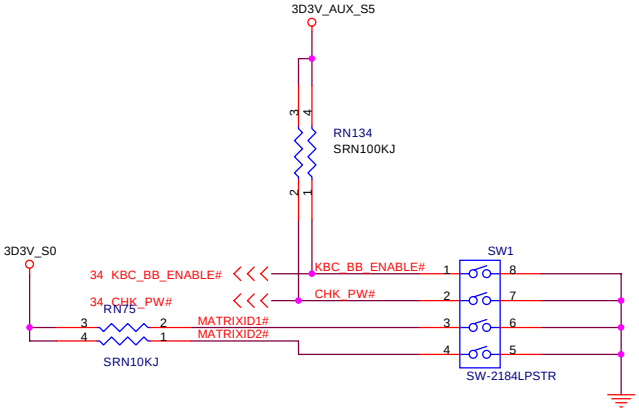
Size: A3 | Document Number: Bolsena | Rev: SA

Date: Tuesday, December 28, 2004 | Sheet 35 of 58



ROM SIZE MAX. 512KBYTE

PLCC32 Socket P/N:
SSKT3262.10002.032
SSKT32 62.10005.032



Keyboard matrix (from vendor)

		US	Jap	Eur	Other
Low Bit	MATRIXID1#	1	1	0	0
High Bit	MATRIXID2#	1	0	1	0

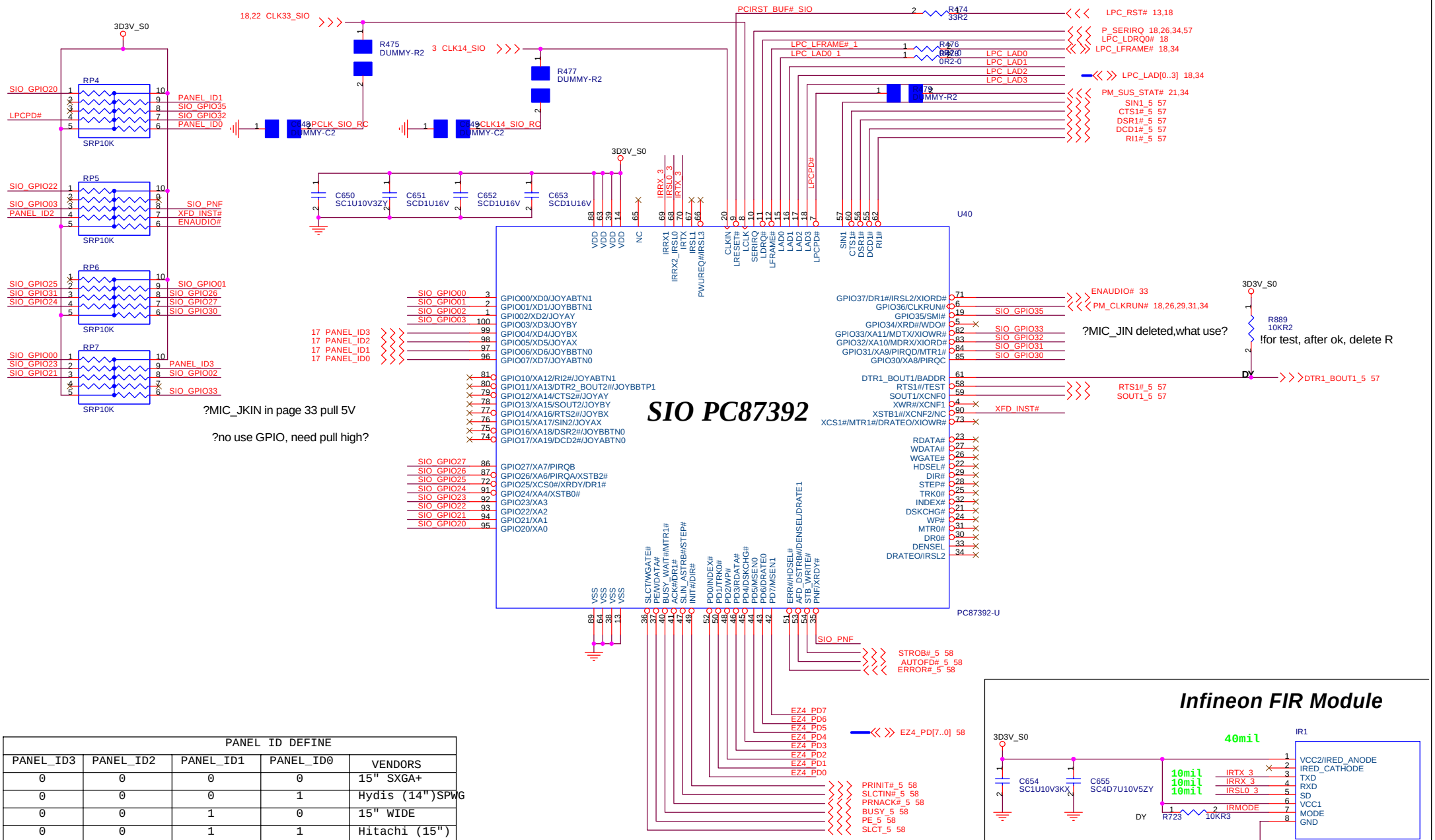
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **BIOS ROM**

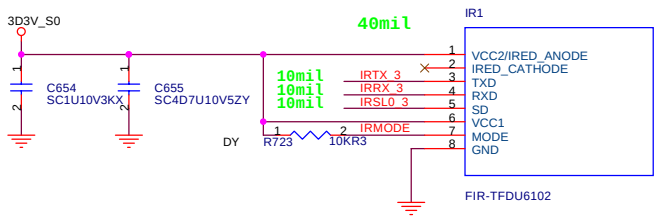
Size: A3 | Document Number: **Bolsena** | Rev: SA

Date: Tuesday, December 28, 2004 | Sheet 36 of 58



PANEL ID DEFINE				
PANEL_ID3	PANEL_ID2	PANEL_ID1	PANEL_ID0	VENDORS
0	0	0	0	15" SXGA+
0	0	0	1	Hydis (14")SPWG
0	0	1	0	15" WIDE
0	0	1	1	Hitachi (15")
0	0	1	1	AU (15")
0	0	1	1	CMO(15")
0	1	0	0	CMO(14")
0	1	0	1	AU (14")
0	1	1	0	AU (14")**
0	1	1	1	No Panel
Note : AU (友達),CMO(奇美),** : With Digitizer				

Infineon FIR Module



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **SUPER IO NC87392**

Size: A3 | Document Number: **Bolsena** | Rev: SA

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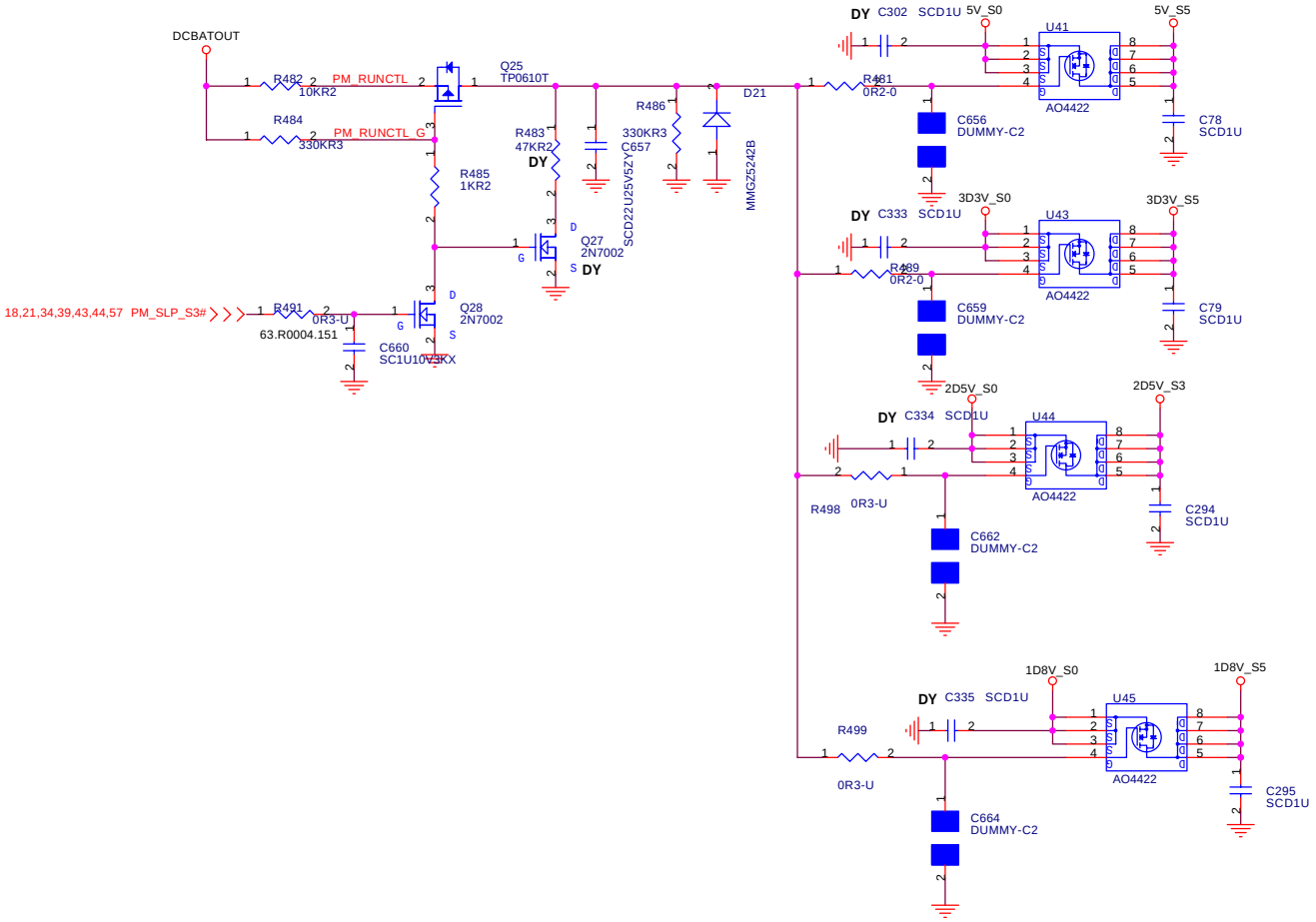
Run Power



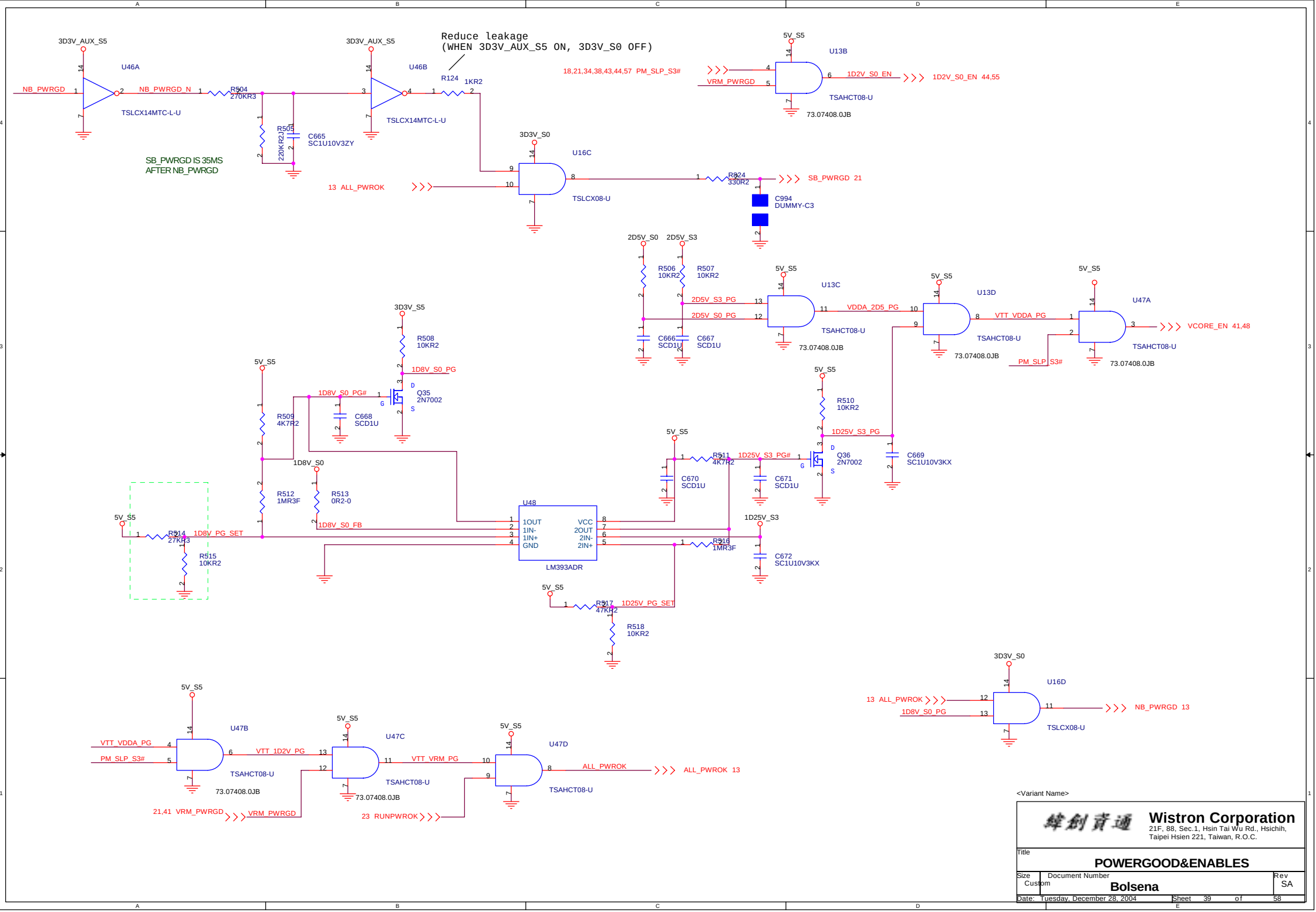
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PWR CTL LOGIC / PWR PLANE**

Size: A3 | Document Number: **Bolsena** | Rev: SA

Date: Tuesday, December 28, 2004 | Sheet 38 of 58



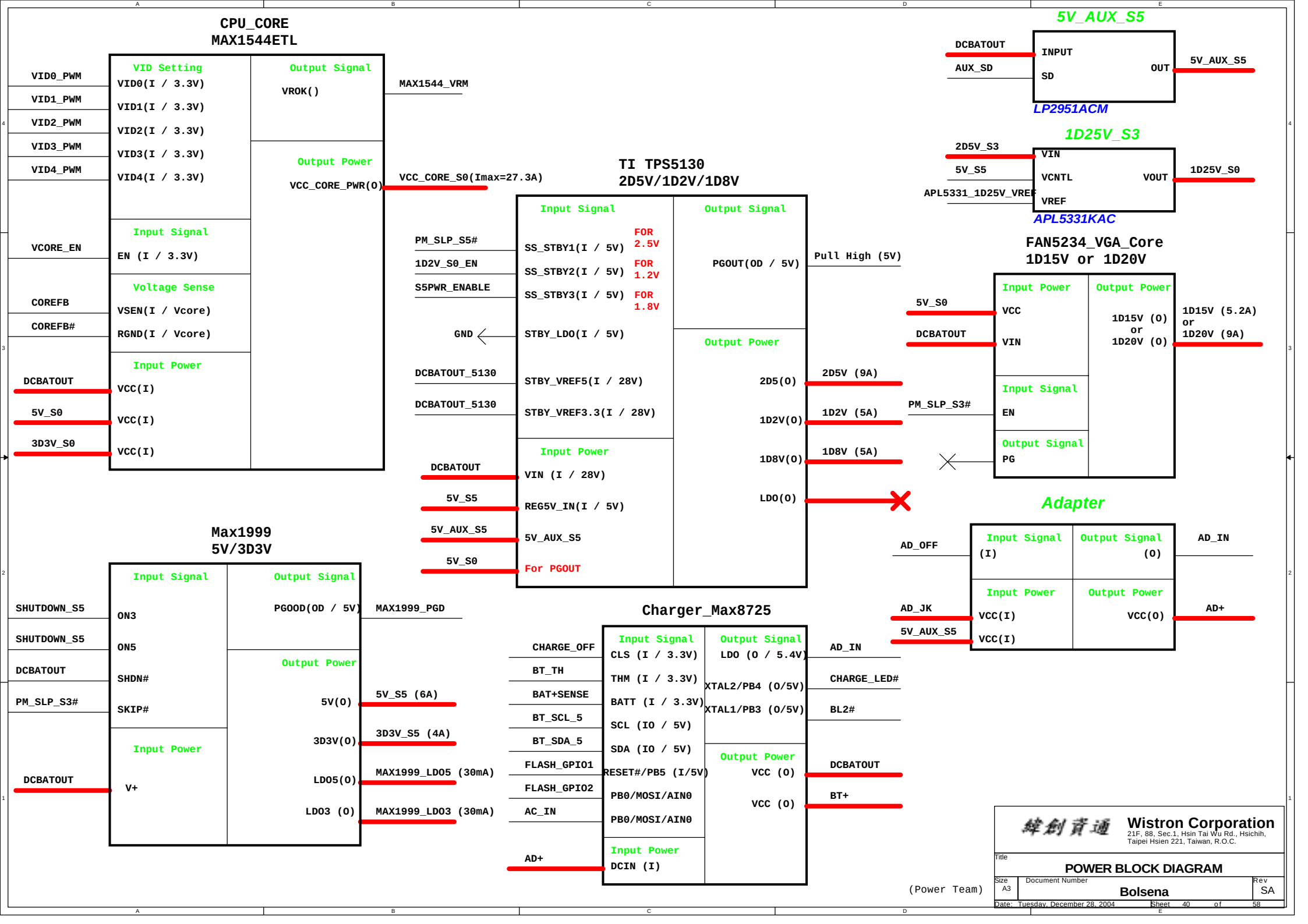
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **POWERGOOD&ENABLES**

Size: Custom | Document Number: **Bolsena** | Rev: SA

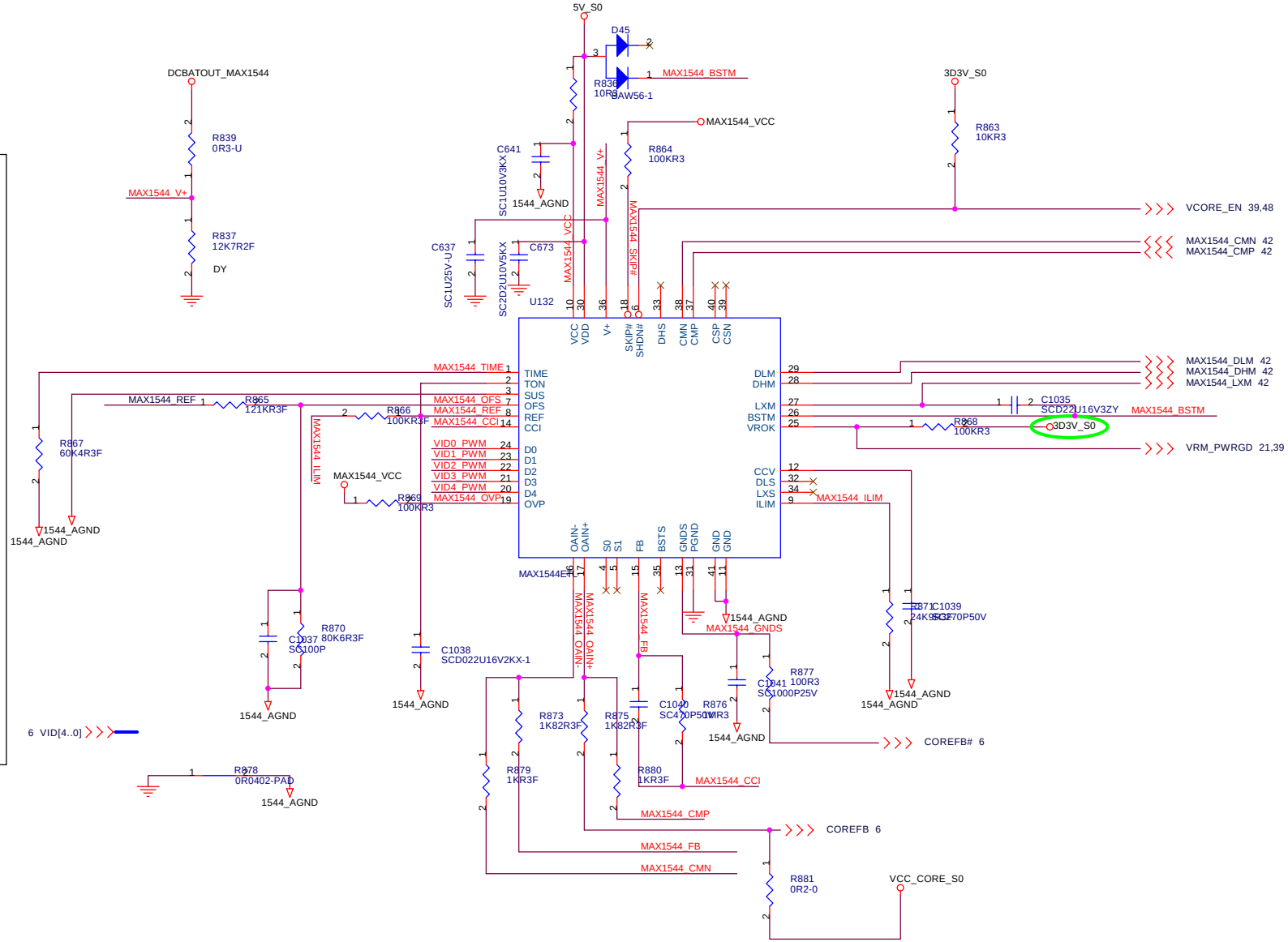
Date: Tuesday, December 28, 2004 | Sheet 39 of 58


CPU_CORE
MAX1544ETL
VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
Output Signal
VROK()
Output Power
VCC_CORE_PWR(O)
Input Signal
EN (I / 3.3V)
Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)
Input Power
VCC(I)
VCC(I)
VCC(I)
VID0_PWM
VID1_PWM
VID2_PWM
VID3_PWM
VID4_PWM
VCORE_EN
COREFB
COREFB#
DCBATOUT
5V_S0
3D3V_S0
MAX1544_VRM
VCC_CORE_S0(Imax=27.3A)
TI TPS5130
2D5V/1D2V/1D8V
Input Signal
SS_STBY1(I / 5V)
SS_STBY2(I / 5V)
SS_STBY3(I / 5V)
STBY_LDO(I / 5V)
STBY_VREF5(I / 28V)
STBY_VREF3.3(I / 28V)
FOR 2.5V
FOR 1.2V
FOR 1.8V
Input Power
VIN (I / 28V)
REG5V_IN(I / 5V)
5V_AUX_S5
For PGOUT
Output Signal
PGOUT(OD / 5V)
Output Power
2D5(O)
1D2V(O)
1D8V(O)
LDO(O)
PM_SLP_S5#
1D2V_S0_EN
S5PWR_ENABLE
GND
DCBATOUT_5130
DCBATOUT_5130
DCBATOUT
5V_S5
5V_AUX_S5
5V_S0
Pull High (5V)
2D5V (9A)
1D2V (5A)
1D8V (5A)
5V_AUX_S5
DCBATOUT
AUX_SD
INPUT
SD
OUT
LP2951ACM
1D25V_S3
2D5V_S3
5V_S5
APL5331_1D25V_VREF
VIN
VCNTL
VREF
VOUT
APL5331KAC
1D25V_S0
FAN5234_VGA_Core
1D15V or 1D20V
Input Power
VCC
VIN
Input Signal
EN
Output Signal
PG
Output Power
1D15V (O)
or
1D20V (O)
5V_S0
DCBATOUT
PM_SLP_S3#
1D15V (5.2A)
or
1D20V (9A)
Adapter
Input Signal
(I)
Output Signal
(O)
Input Power
VCC(I)
VCC(I)
Output Power
VCC(O)
AD_OFF
AD_JK
5V_AUX_S5
AD_IN
AD+
Max1999
5V/3D3V
Input Signal
ON3
ON5
SHDN#
SKIP#
Input Power
V+
Output Signal
PGOOD(OD / 5V)
Output Power
5V(O)
3D3V(O)
LDO5(O)
LDO3 (O)
SHUTDOWN_S5
SHUTDOWN_S5
DCBATOUT
PM_SLP_S3#
DCBATOUT
MAX1999_PGD
5V_S5 (6A)
3D3V_S5 (4A)
MAX1999_LDO5 (30mA)
MAX1999_LDO3 (30mA)
Charger_Max8725
Input Signal
CLS (I / 3.3V)
THM (I / 3.3V)
BATT (I / 3.3V)
SCL (IO / 5V)
SDA (IO / 5V)
RESET#/PB5 (I/5V)
PB0/MOSI/AIN0
PB0/MOSI/AIN0
Input Power
DCIN (I)
Output Signal
LDO (O / 5.4V)
XTAL2/PB4 (O/5V)
XTAL1/PB3 (O/5V)
Output Power
VCC (O)
VCC (O)
CHARGE_OFF
BT_TH
BAT+SENSE
BT_SCL_5
BT_SDA_5
FLASH_GPIO1
FLASH_GPIO2
AC_IN
AD+
AD_IN
CHARGE_LED#
BL2#
DCBATOUT
BT+
(Power Team)
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
POWER BLOCK DIAGRAM
Size
A3
Document Number
Bolsena
Rev
SA
Date: Tuesday, December 28, 2004
Sheet 40 of 58

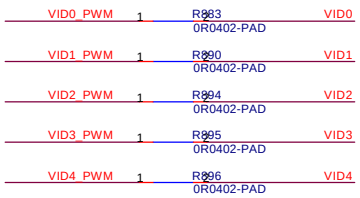
CPU_VCORE
VID=1.20V
Iomax=27.3A (35W)

TABLE 1. VOLTAGE IDENTIFICATION CODES

VID4	VID3	VID2	VID1	VID0	DAC
0	0	0	0	0	1.550
0	0	0	0	1	1.525
0	0	0	1	0	1.500
0	0	0	1	1	1.475
0	0	1	0	0	1.450
0	0	1	0	1	1.425
0	0	1	1	0	1.400
0	0	1	1	1	1.375
0	1	0	0	0	1.350
0	1	0	0	1	1.325
0	1	0	1	0	1.300
0	1	0	1	1	1.275
0	1	1	0	0	1.250
0	1	1	0	1	1.225
0	1	1	1	0	1.200
0	1	1	1	1	1.175
1	0	0	0	0	1.150
1	0	0	0	1	1.125
1	0	0	1	0	1.100
1	0	0	1	1	1.075
1	0	1	0	0	1.050
1	0	1	0	1	1.025
1	0	1	1	0	1.000
1	0	1	1	1	0.975
1	1	0	0	0	0.950
1	1	0	0	1	0.925
1	1	0	1	0	0.900
1	1	0	1	1	0.875
1	1	1	0	0	0.850
1	1	1	0	1	0.825
1	1	1	1	0	0.800
1	1	1	1	1	Shutdown



VCC_CORE_S0 feedback



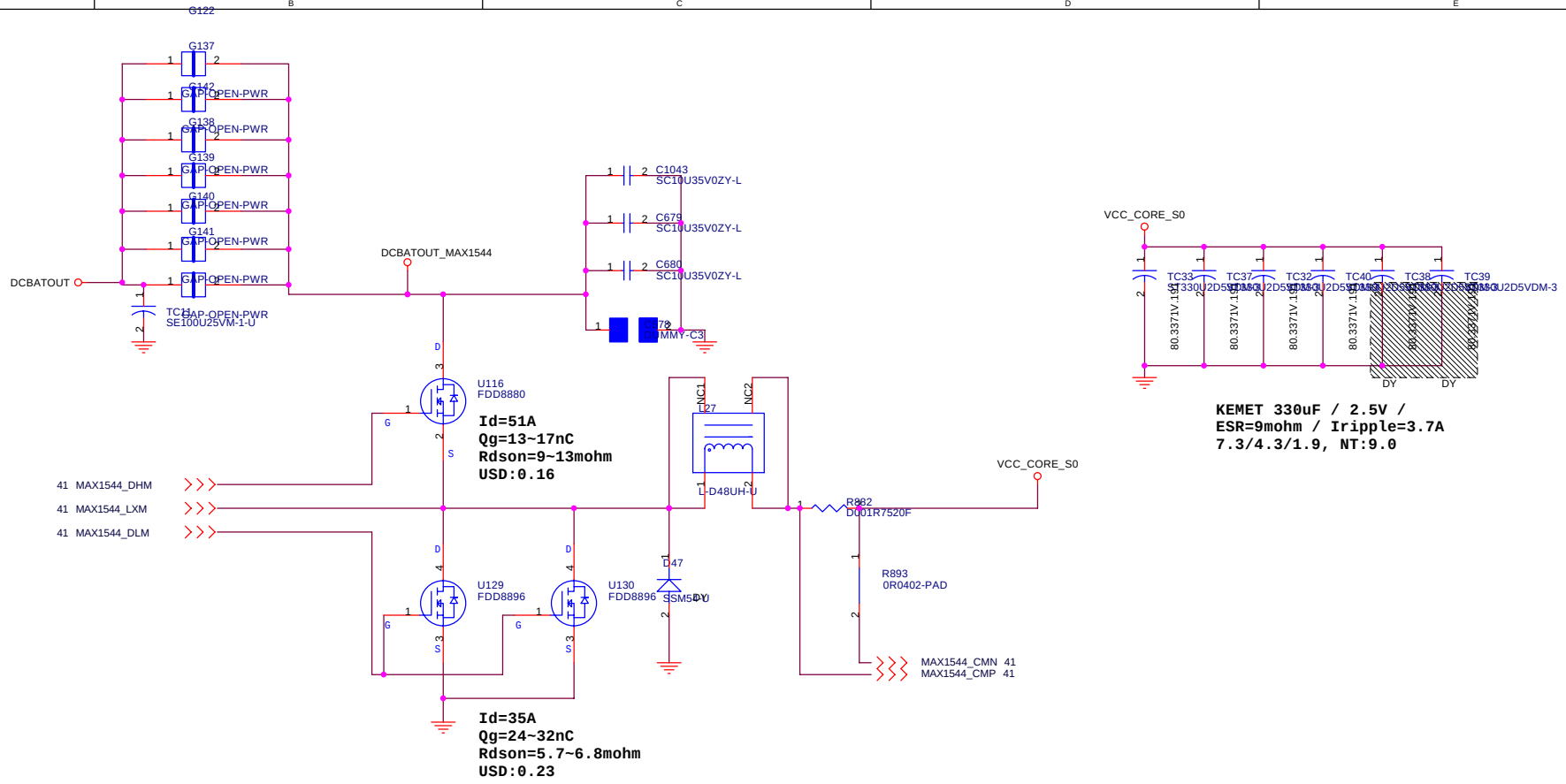
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU Vcore 1

Size: A3 | Document Number: Bolsena | Rev: SA

(Power Team) Date: Tuesday, December 28, 2004 | Sheet 41 of 58



(Power Team)

<Variant Name>

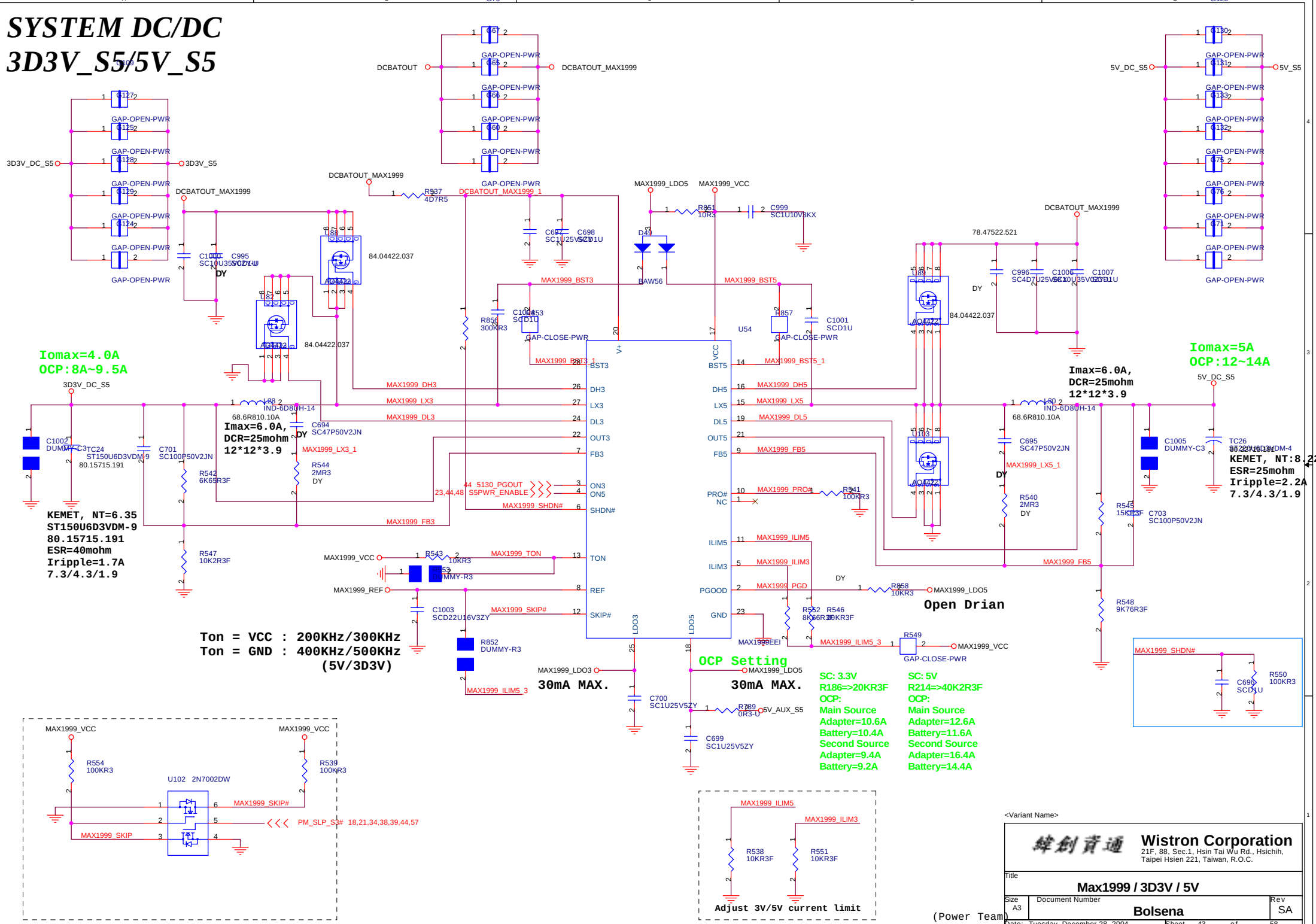
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU Vcore 2**

Size: A3 | Document Number: **Bolsena** | Rev: SA

Date: Tuesday, December 28, 2004 | Sheet 42 of 58

SYSTEM DC/DC
3D3V_S5/5V_S5



TI TPS5130 for 2.5V, 1.2V, 1.8V

Vo=(R1*0.85)/R2+0.85

(2D5V=>CH1 , 1D2V=>CH2 , 1D8V =>CH3)

For 1.8V
SETTING=1.8275V

For 1.2V
SETTING=1.2172V

For 2.5V
SETTING=2.516V

close to IC

T(soft)=1.736ms

PWM_SEL	Condition	Voltage
	H : Auto PWM/SKIP	2.2V(Min)~
	* L : PWM fixed (300KHz)	~0.3V(Max)

2D5V_OCP
OCP
12A=>R225=18K
18A=>R225=28K

1D2V_OCP
OCP
8.4A=>R226=13K
10A=>R226=22K

1D8V_OCP
OCP
8.4A=>R229=12.65K
10A=>R229=22K

TPS5130

LDO SETTING

PWM_SEL	Condition	Voltage
	H : Auto PWM/SKIP	2.2V(Min)~
	* L : PWM fixed (300KHz)	~0.3V(Max)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

<Variant Name>

Title: TPS5130 1D2V/1D8V2D5V/ (1/2)

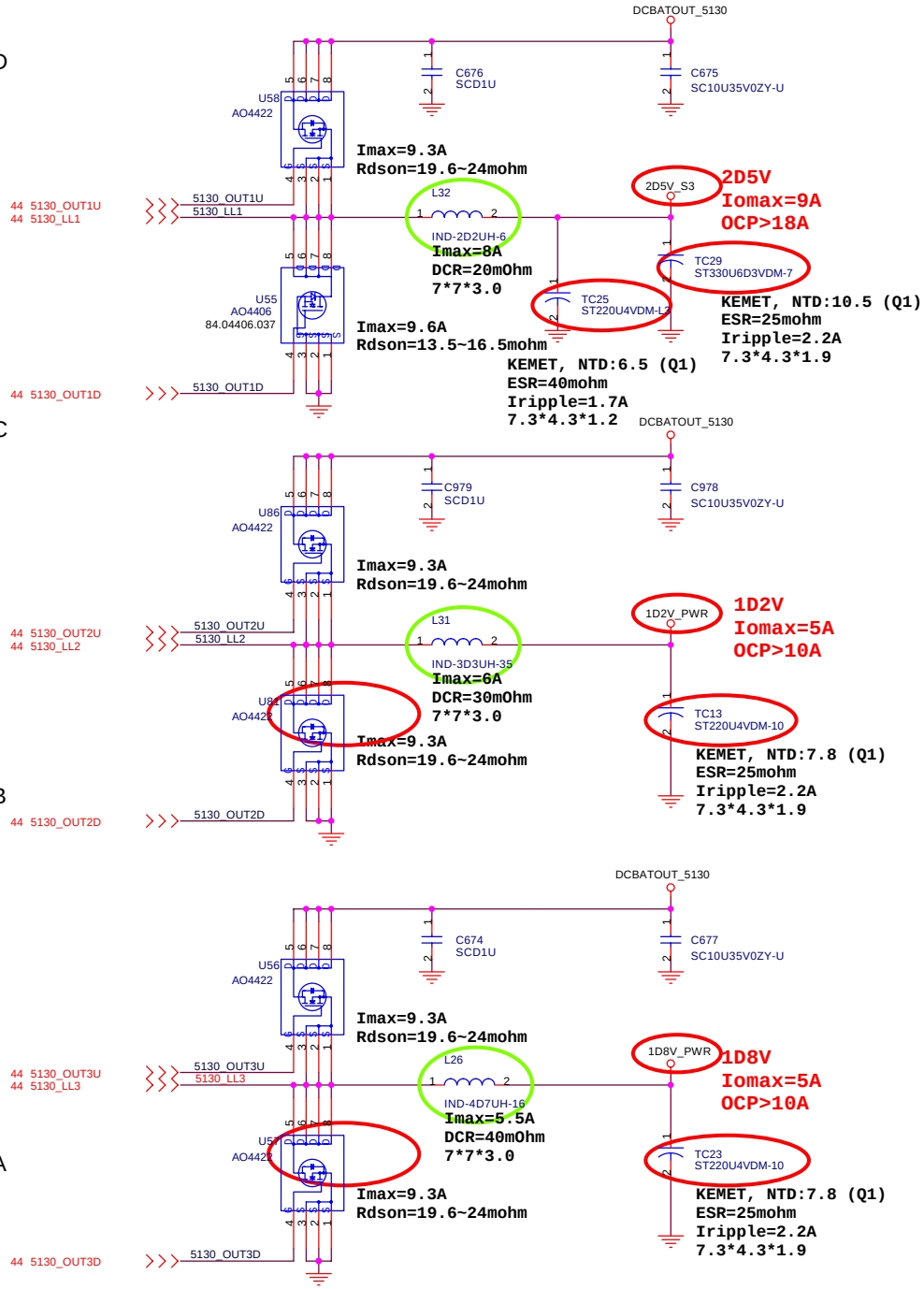
Size: A3 | Document Number: Bolsena | Rev: SA

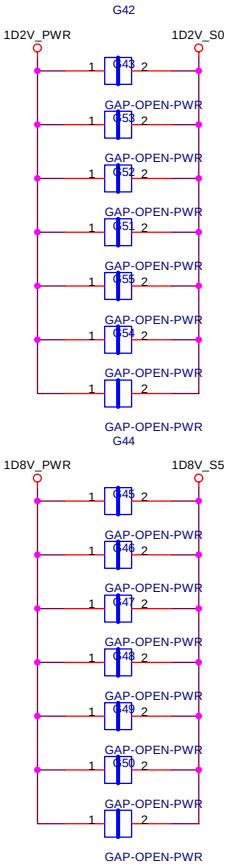
Date: Tuesday, December 28, 2004 | Sheet 44 of 58

(Power Team)

TI TPS5130 for 2D5V, 1D2V, 1D8V

(2D5V=>CH1 , 1D2V=>CH2 , 1D8V =>CH3)





(Power Team)

<Variant Name>

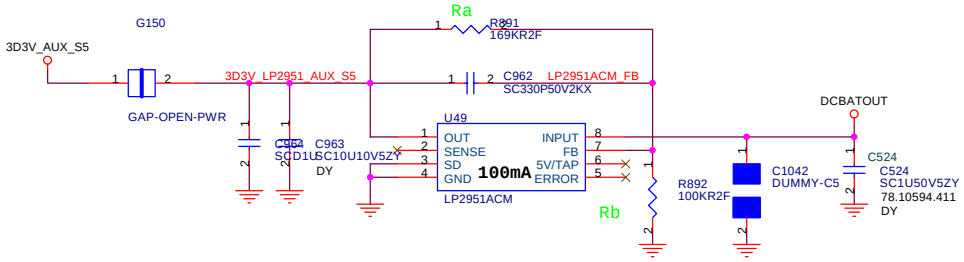
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS5130 1D2V/1D8V2D5V/ (2/2)

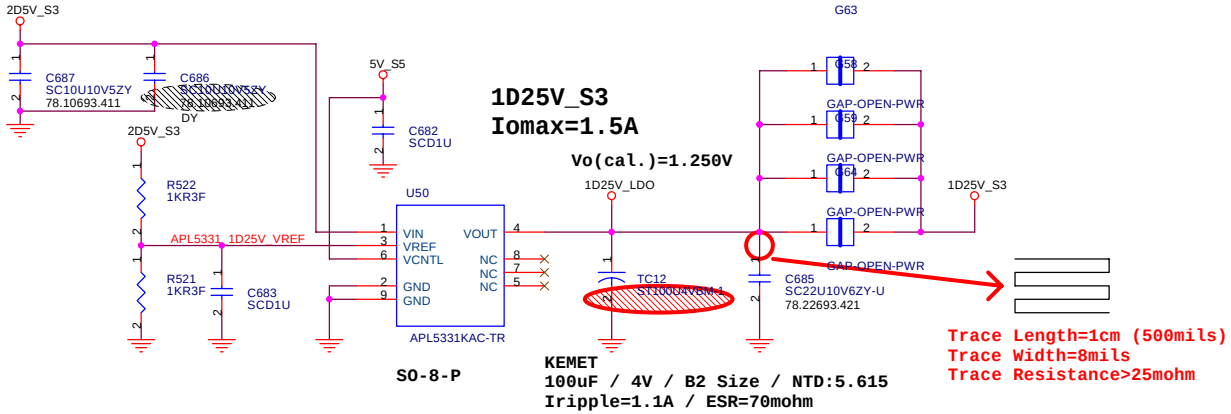
Size: A3 | Document Number: Bolsena | Rev: SA

Date: Tuesday, December 28, 2004 | Sheet 45 of 58

3D3V_AUX_S5

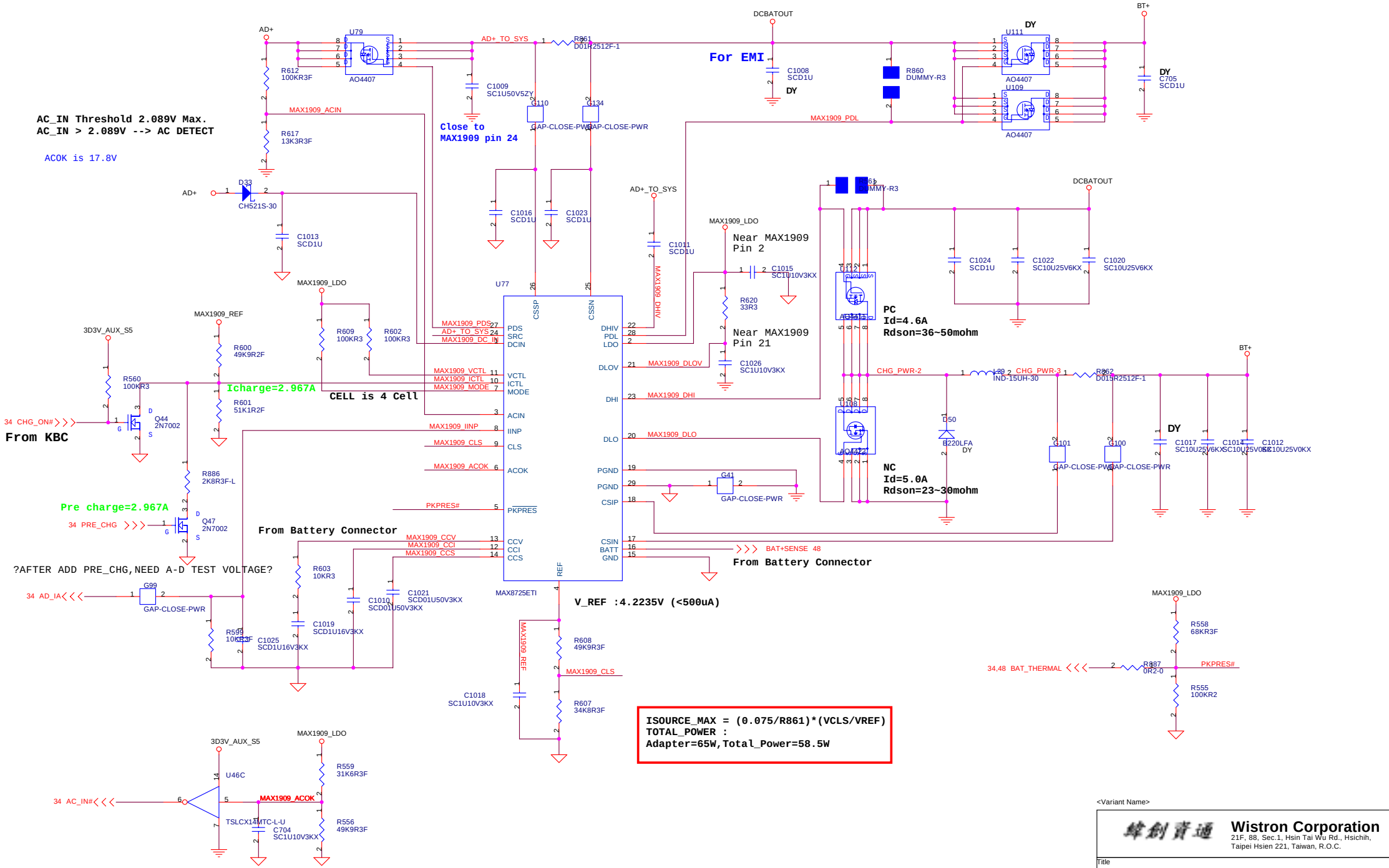


Vout = 1.23 * (Ra / Rb)

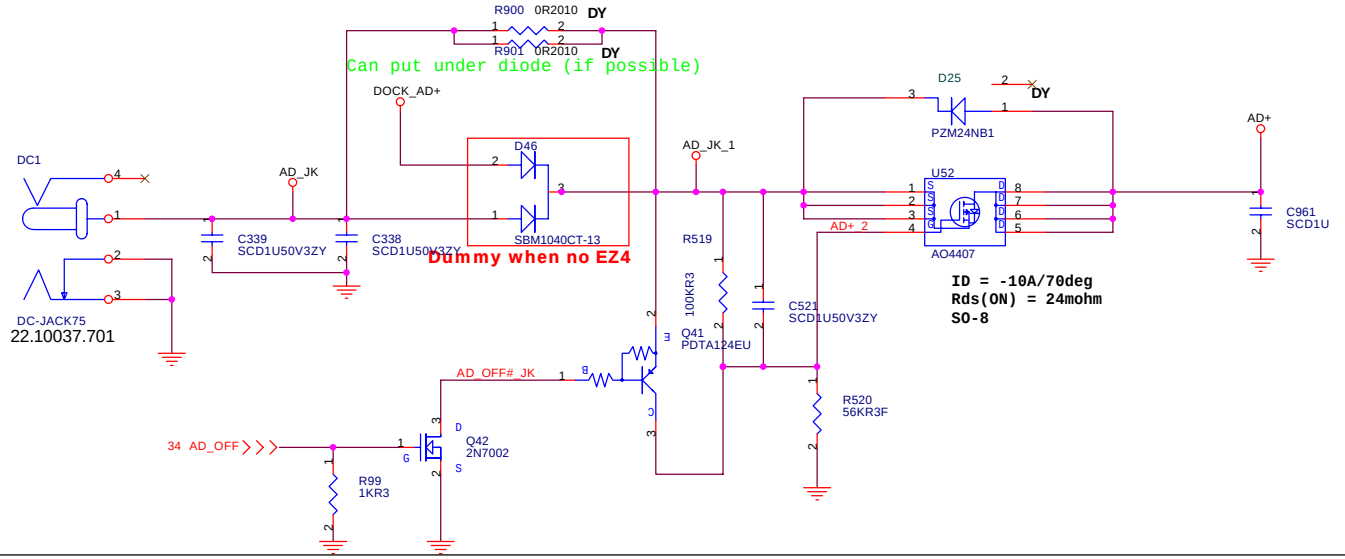


(Power Team)

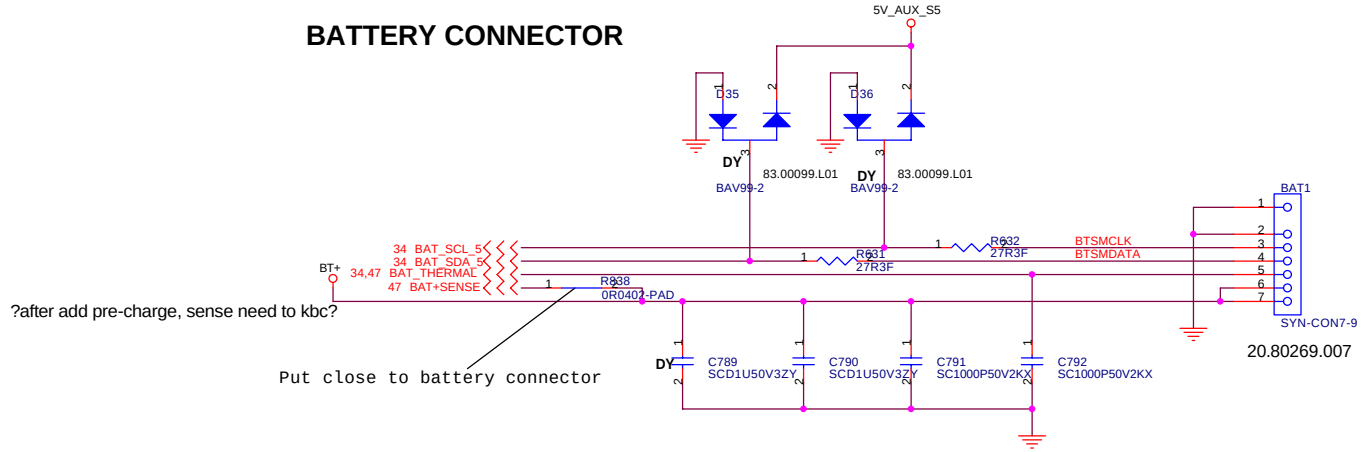
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**1D2V_S3 / 3D3V_AUX**	
Size A3	Document Number **Bolsena**	Rev SA
Date: Tuesday, December 28, 2004	Sheet 46 of 58	


AC_IN Threshold 2.089V Max.
AC_IN > 2.089V --> AC DETECT
ACOK is 17.8V
Close to MAX1909 pin 24
For EMI
Near MAX1909 Pin 2
Near MAX1909 Pin 21
PC
Id=4.6A
Rdson=36~50mohm
NC
Id=5.0A
Rdson=23~30mohm
Icharge=2.967A
CELL is 4 Cell
From KBC
Pre charge=2.967A
From Battery Connector
?AFTER ADD PRE_CHG,NEED A-D TEST VOLTAGE?
V_REF :4.2235V (<500uA)
ISOURCE_MAX = (0.075/R861)*(VCLS/VREF)
TOTAL_POWER :
Adapter=65W,Total_Power=58.5W
MAX8725ETI
U77
DCBATOUT
BT+
AD+
3D3V_AUS_S5
MAX1909_LDO
MAX1909_REF
AD+_TO_SYS
MAX1909_ACIN
MAX1909_PDL
CHG_PWR-2
CHG_PWR-3
BAT+SENSE 48
34,48 BAT_THERMAL
34 CHG_ON#
34 PRE_CHG
34 AD_IA
34 AC_IN#
PKPRES#
MAX1909_ACOK
MAX1909_CLS
MAX1909_DLOV
MAX1909_DHI
MAX1909_DLO
MAX1909_VCTL
MAX1909_ICTL
MAX1909_MODE
MAX1909_IINP
MAX1909_CCV
MAX1909_CCI
MAX1909_CCS
MAX1909_PDS
MAX1909_DC_IN
MAX1909_DHIV
MAX1909_REF
DY
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CHARGER MAX8725
Size Custom
Document Number
Bolsena
Rev
SA
Date: Tuesday, December 28, 2004
Sheet 47 of 58
(Power Team)

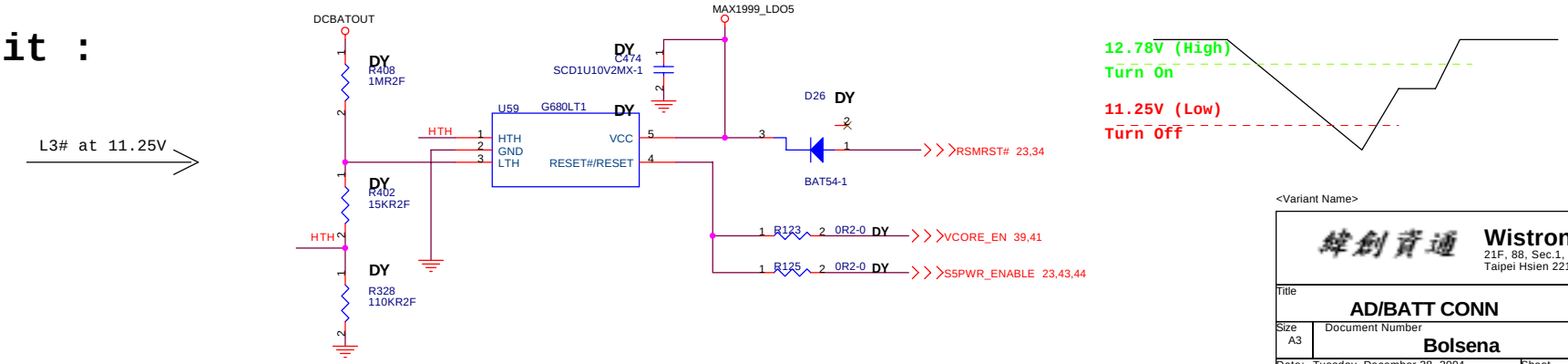
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR

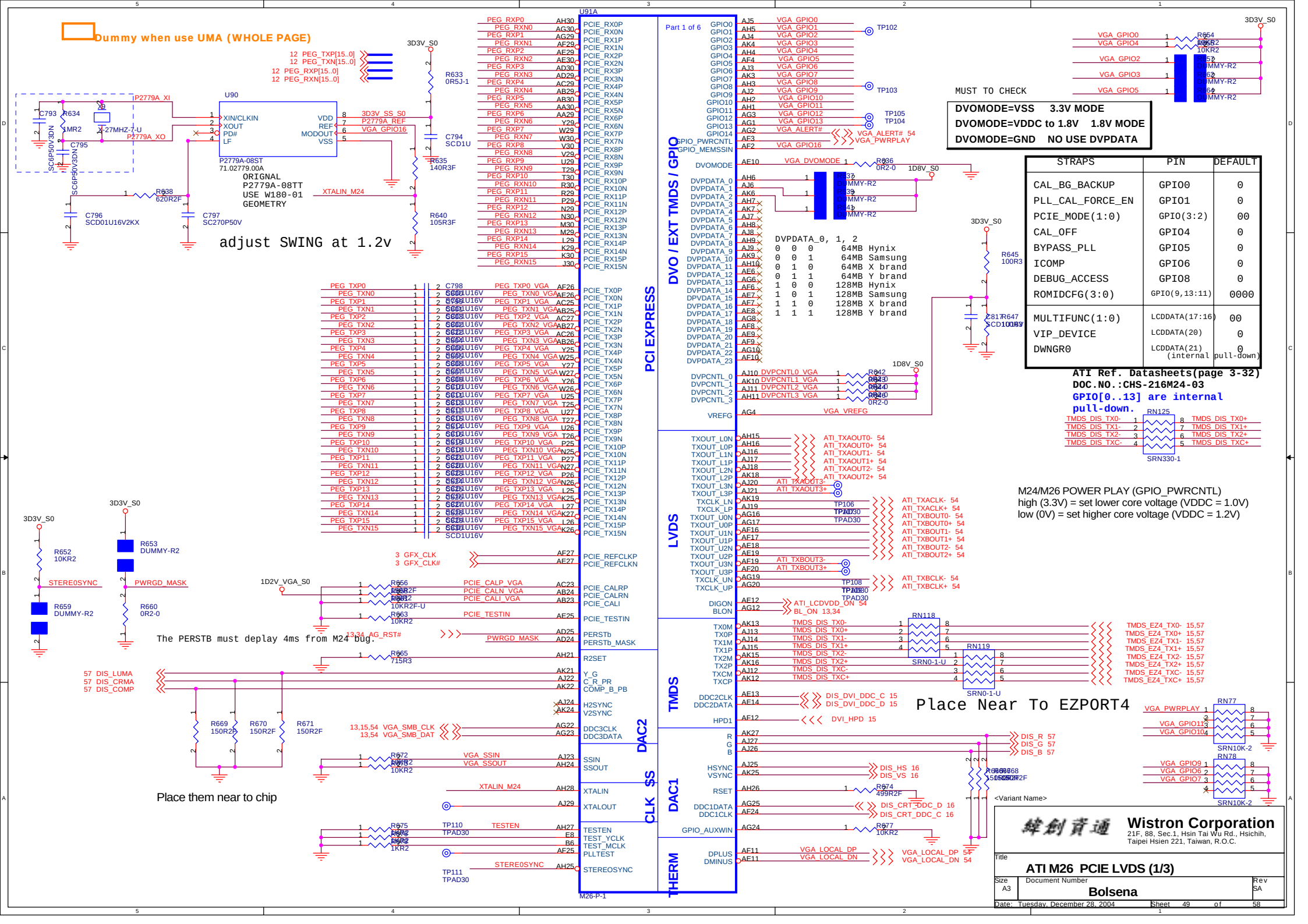


Low3 Circuit :



<Variant Name>

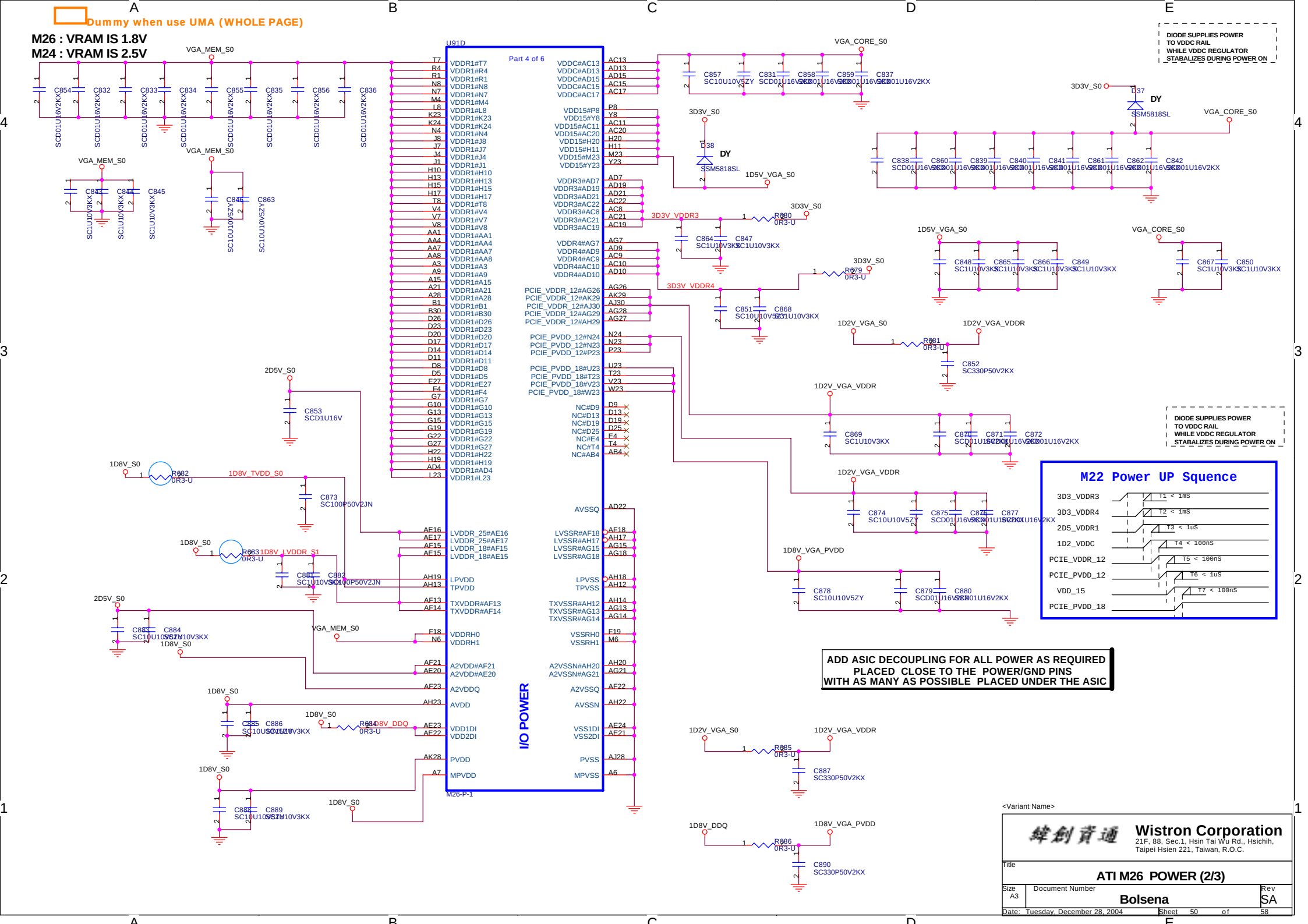
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**AD/BATT CONN**	
Size A3	Document Number **Bolsena**	Rev SA
Date: Tuesday, December 28, 2004	Sheet 48 of 58	



STRAPS	PIN	DEFAULT
CAL_BG_BACKUP	GPIO0	0
PLL_CAL_FORCE_EN	GPIO1	0
PCIE_MODE(1:0)	GPIO(3:2)	00
CAL_OFF	GPIO4	0
BYPASS_PLL	GPIO5	0
ICOMP	GPIO6	0
DEBUG_ACCESS	GPIO8	0
ROMIDCFG(3:0)	GPIO(9,13:11)	0000
MULTIFUNC(1:0)	LCDDATA(17:16)	00
VIP_DEVICE	LCDDATA(20)	0
DWNGR0	LCDDATA(21) (internal pull-down)	0

Dummy when use UMA (WHOLE PAGE)

M26 : VRAM IS 1.8V
M24 : VRAM IS 2.5V



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATI M26 POWER (2/3)**

Size: A3 | Document Number: **Bolsena** | Rev: SA

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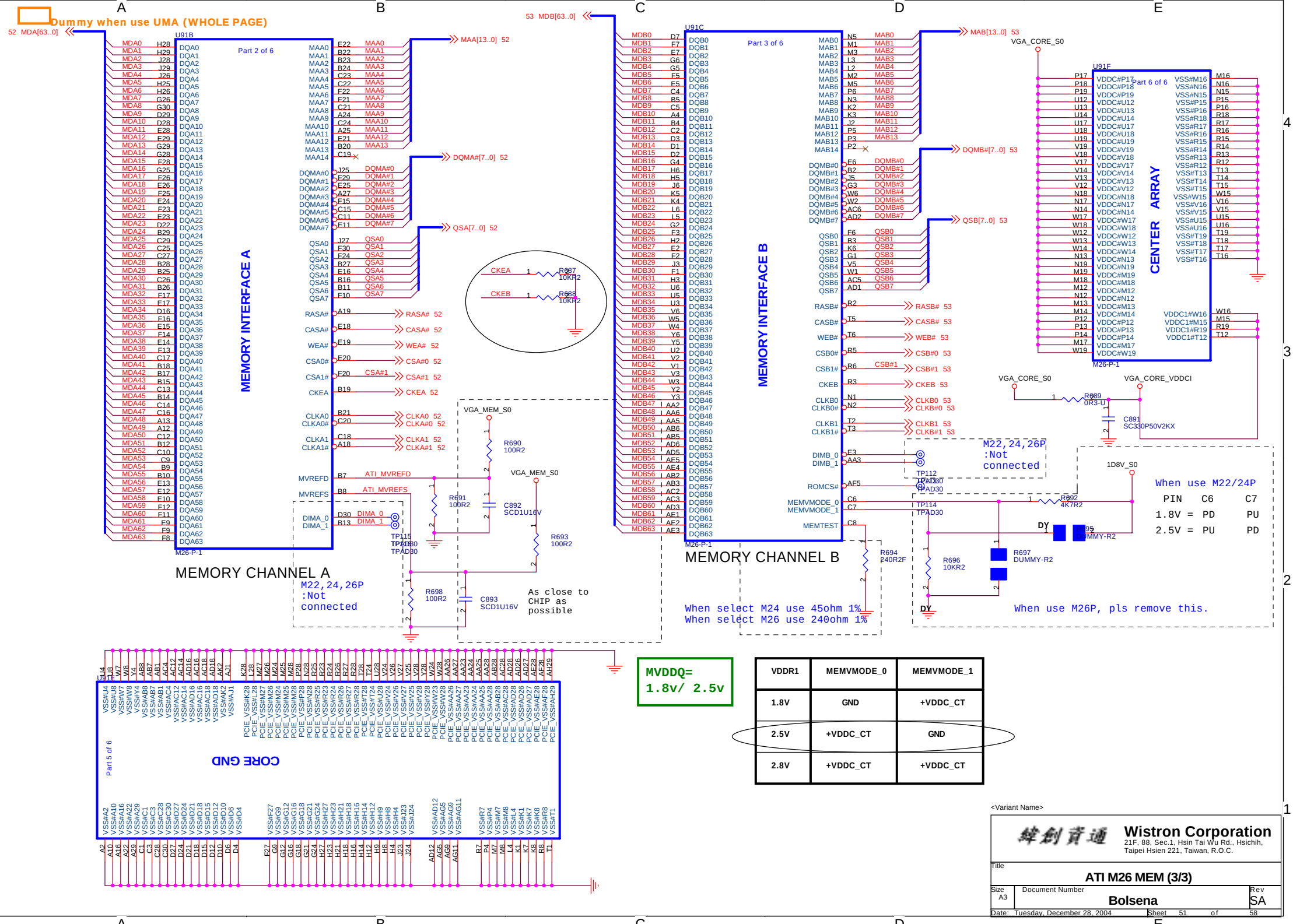

MVDDQ=
1.8v/ 2.5v

VDDR1	MEMVMODE_0	MEMVMODE_1
1.8V	GND	+VDDC_CT
2.5V	+VDDC_CT	GND
2.8V	+VDDC_CT	+VDDC_CT

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI M26 MEM (3/3)

Size: A3 | Document Number: Bolsena | Rev: SA

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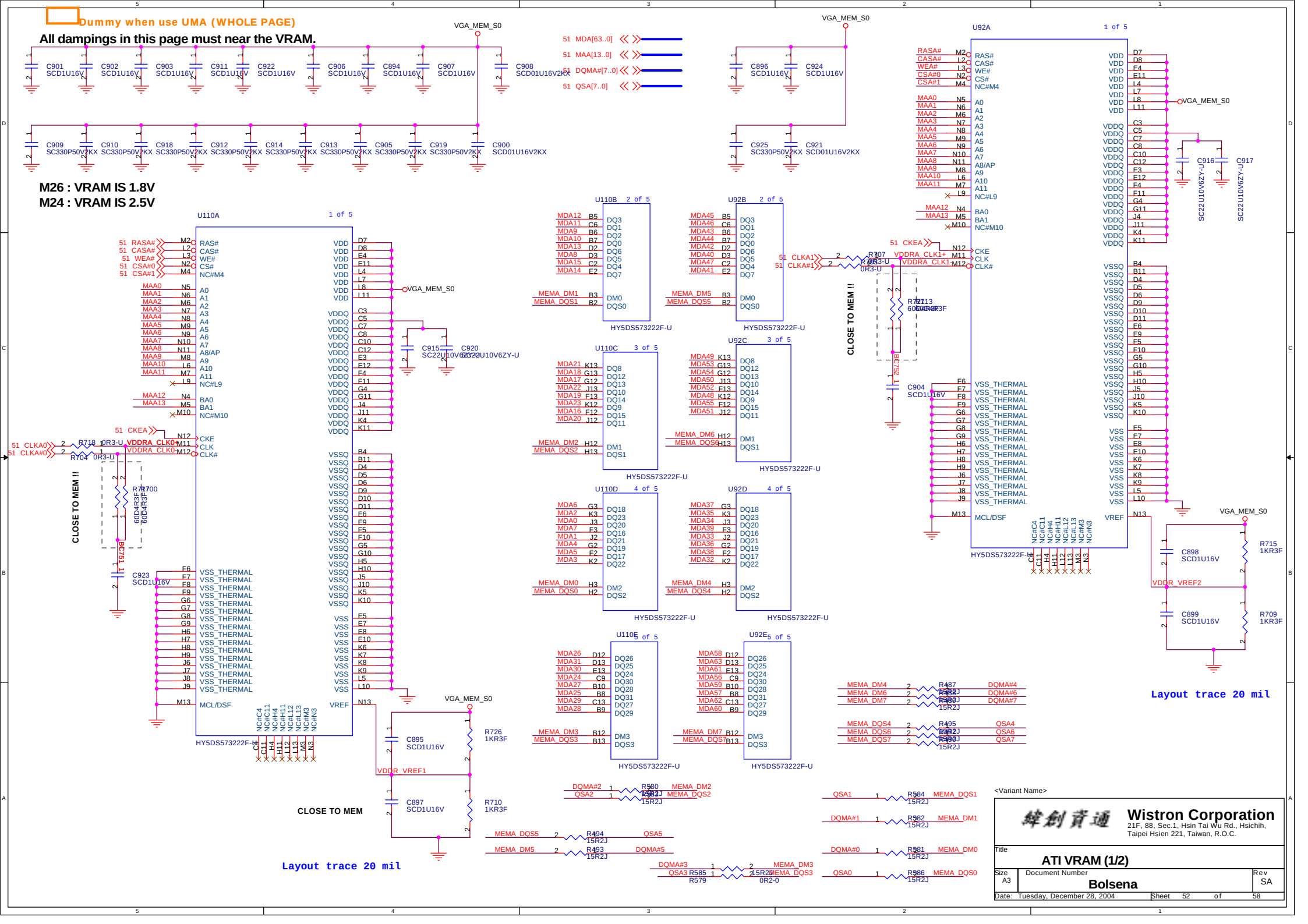
Dummy when use UMA (WHOLE PAGE)

All dampings in this page must near the VRAM.

M26 : VRAM IS 1.8V
M24 : VRAM IS 2.5V



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATI VRAM (1/2)**

Size	Document Number	Rev
A3	**Bolsena**	SA

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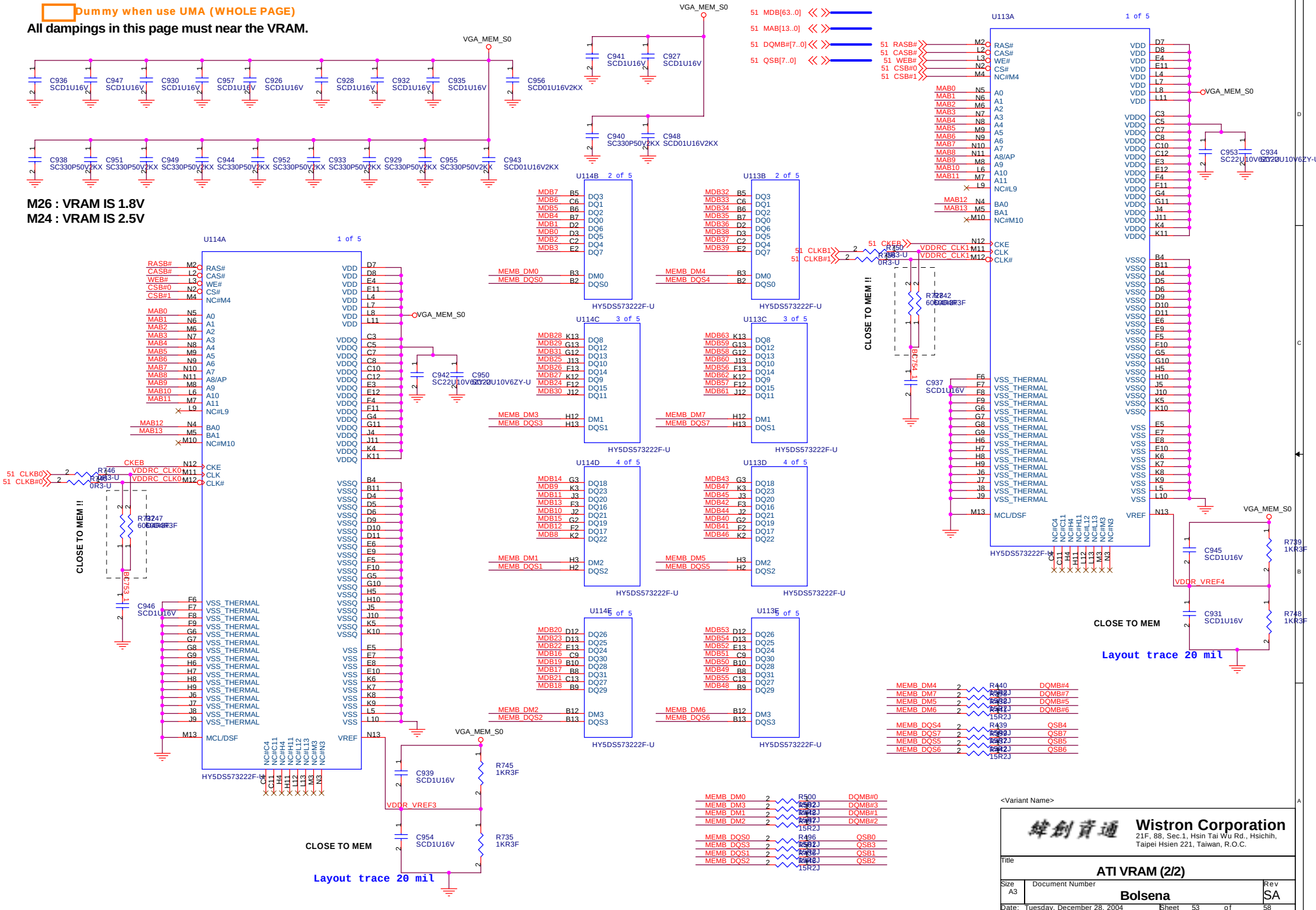
Dummy when use UMA (WHOLE PAGE)

All dampings in this page must near the VRAM.



M26 : VRAM IS 1.8V
M24 : VRAM IS 2.5V

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

<Variant Name>

Title: **ATI VRAM (2/2)**

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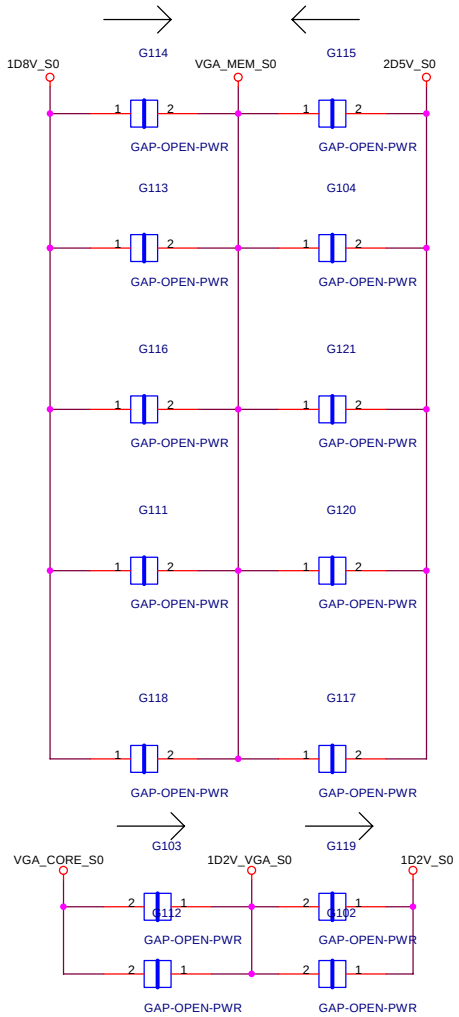
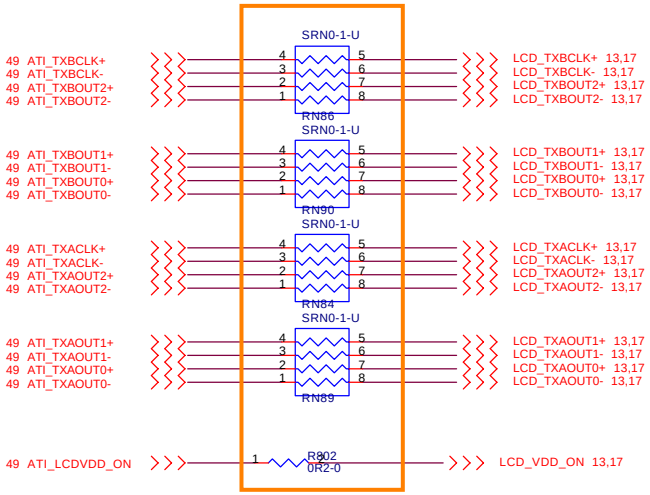
Date: Tuesday, December 28, 2004 | Sheet 53 of 58

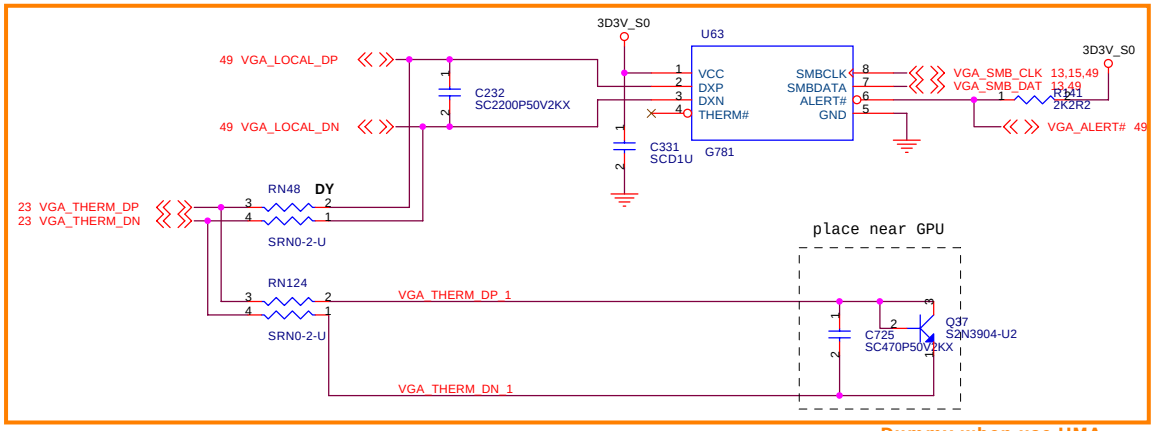
M26 : VRAM IS 1.8V
M24 : VRAM IS 2.5V

ONLY 1.8 'OR' 2.5 SHORT





Dummy when use UMA



Dummy when use UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
VGA SELECTOR		
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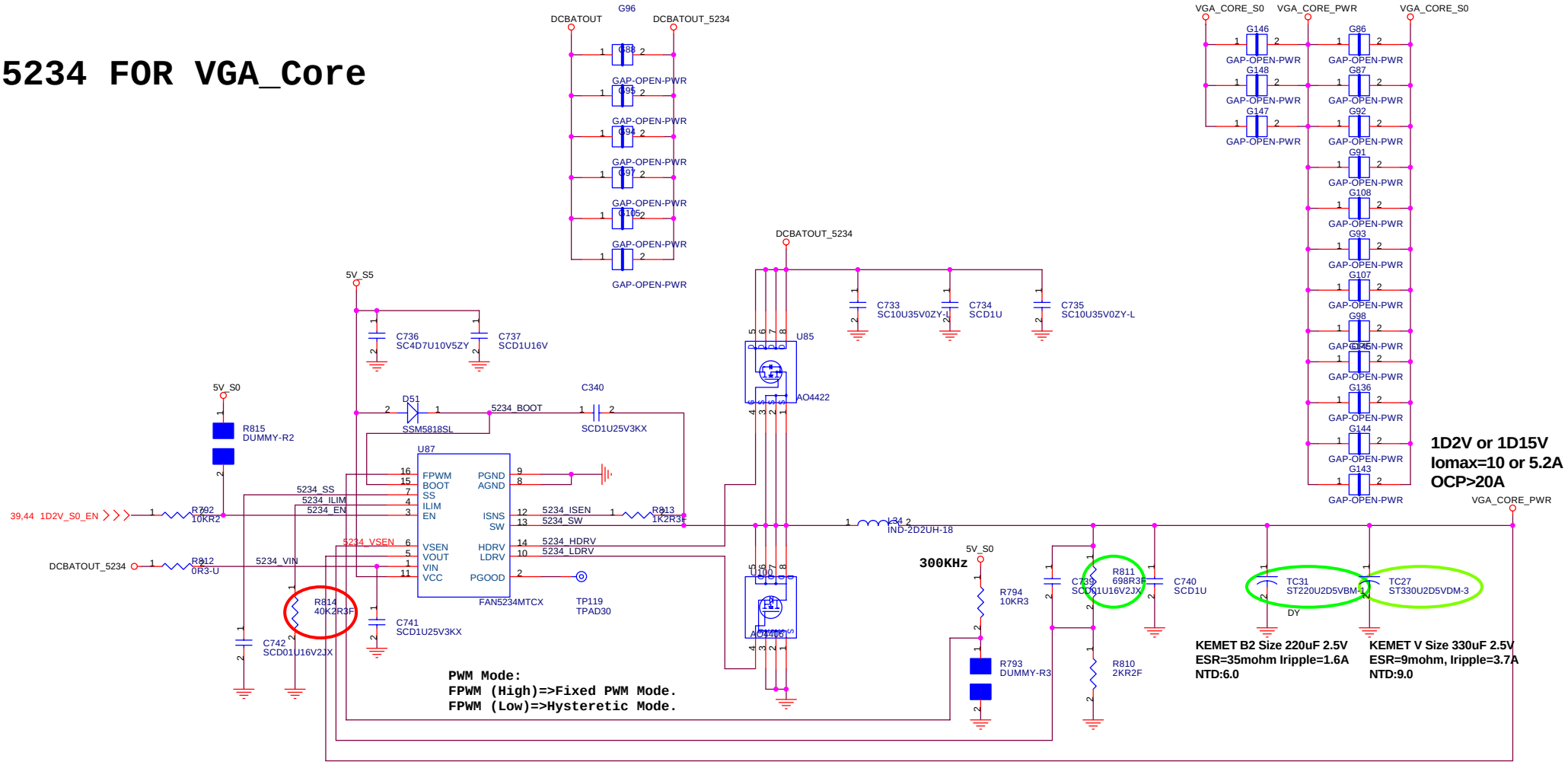
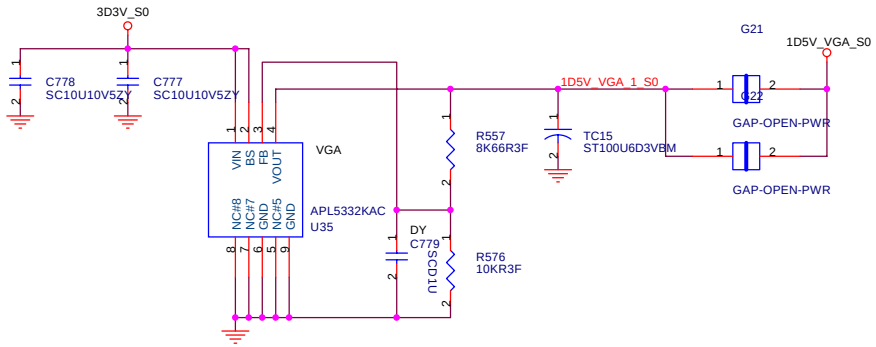
FAN5234 FOR VGA_Core



?M24/M26 POWER PLAY (GPIO_PWRCNTL)
high (3.3V) = set lower core voltage (VDDC = 1.0V)
low (0V) = set higher core voltage (VDDC = 1.2V)



(Power Team)

<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**VGA CORE 1D2V or 1D0V**	
Size A3	Document Number **Bolsena**	Rev SA
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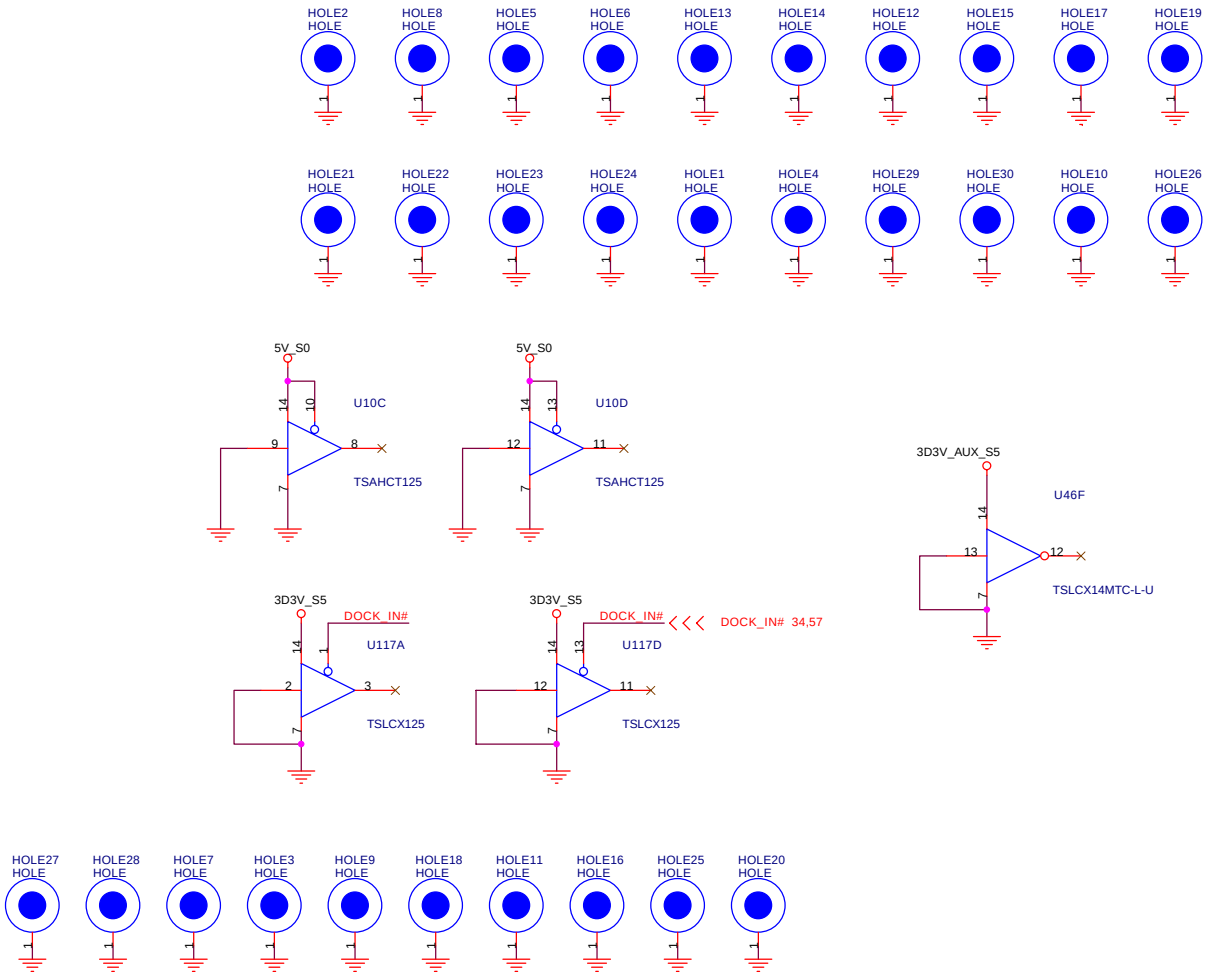

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **EMI**

Size	Document Number	Rev
A3	**Bolsena**	SA

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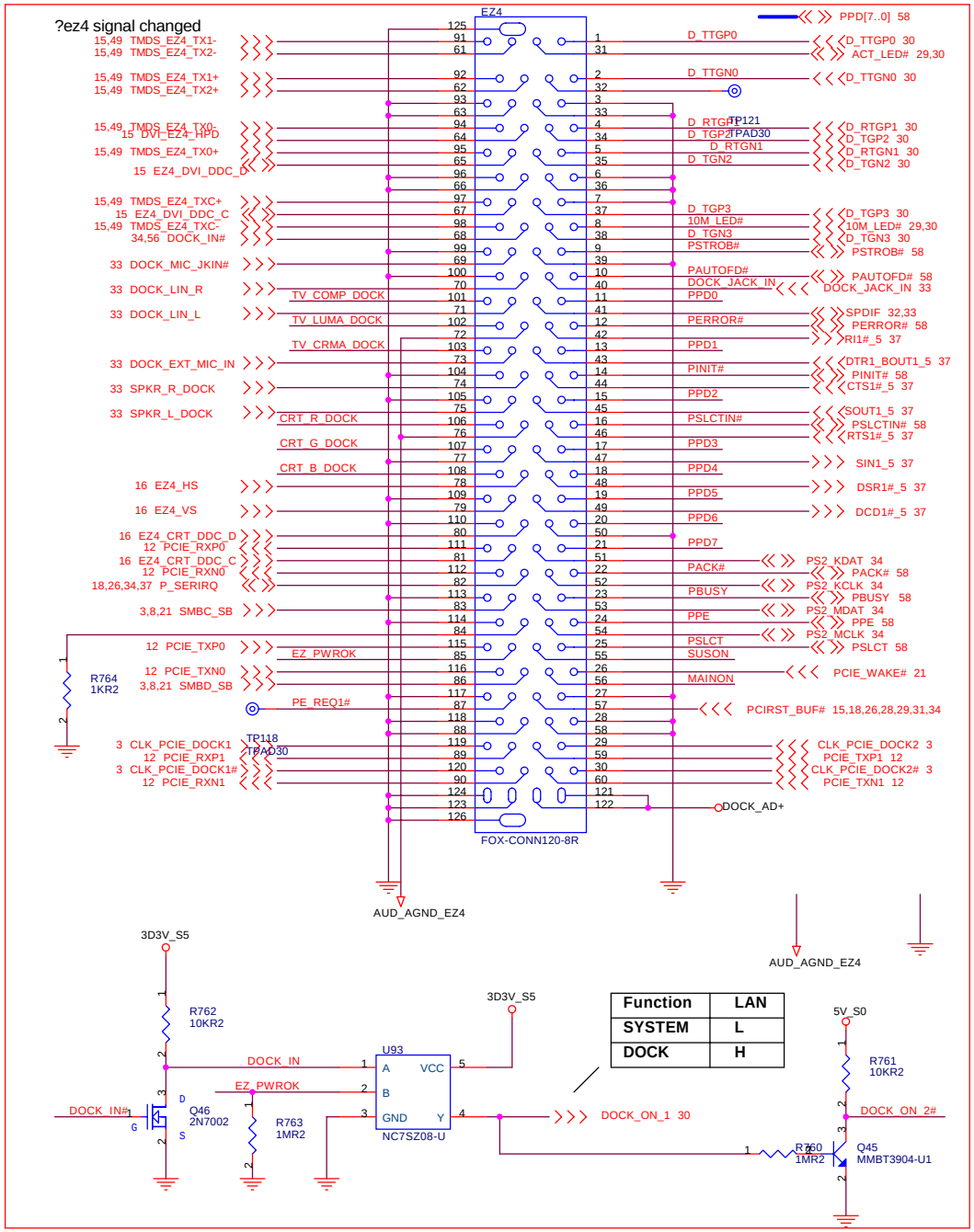
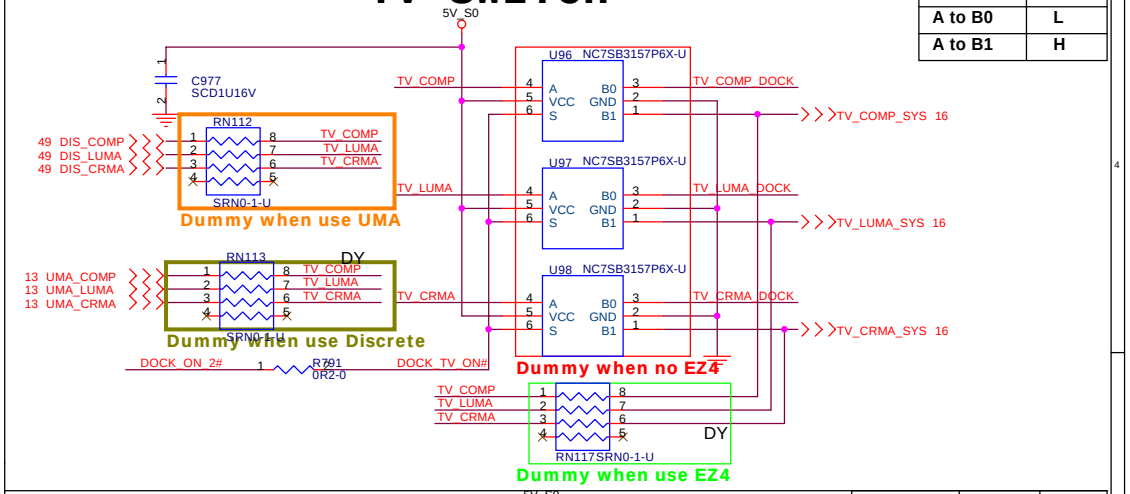


Function	LAN
SYSTEM	L
DOCK	H

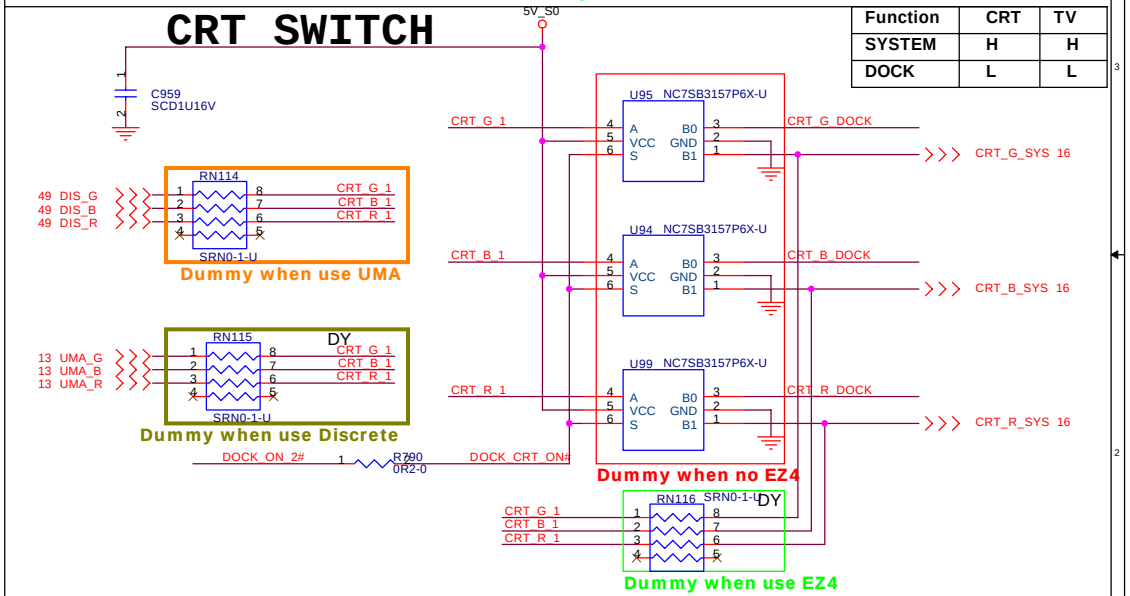
TV SWITCH

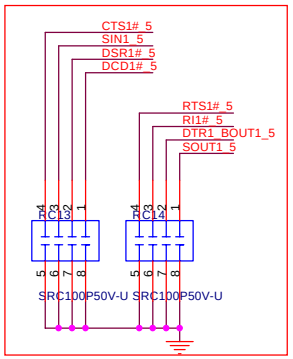
Function	S
A to B0	L
A to B1	H

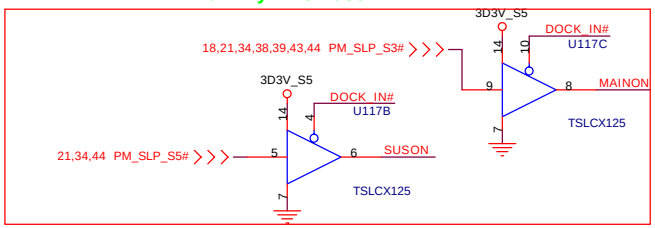


CRT SWITCH

Function	CRT	TV
SYSTEM	H	H
DOCK	L	L







<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: EASY PORT4 (1/2)

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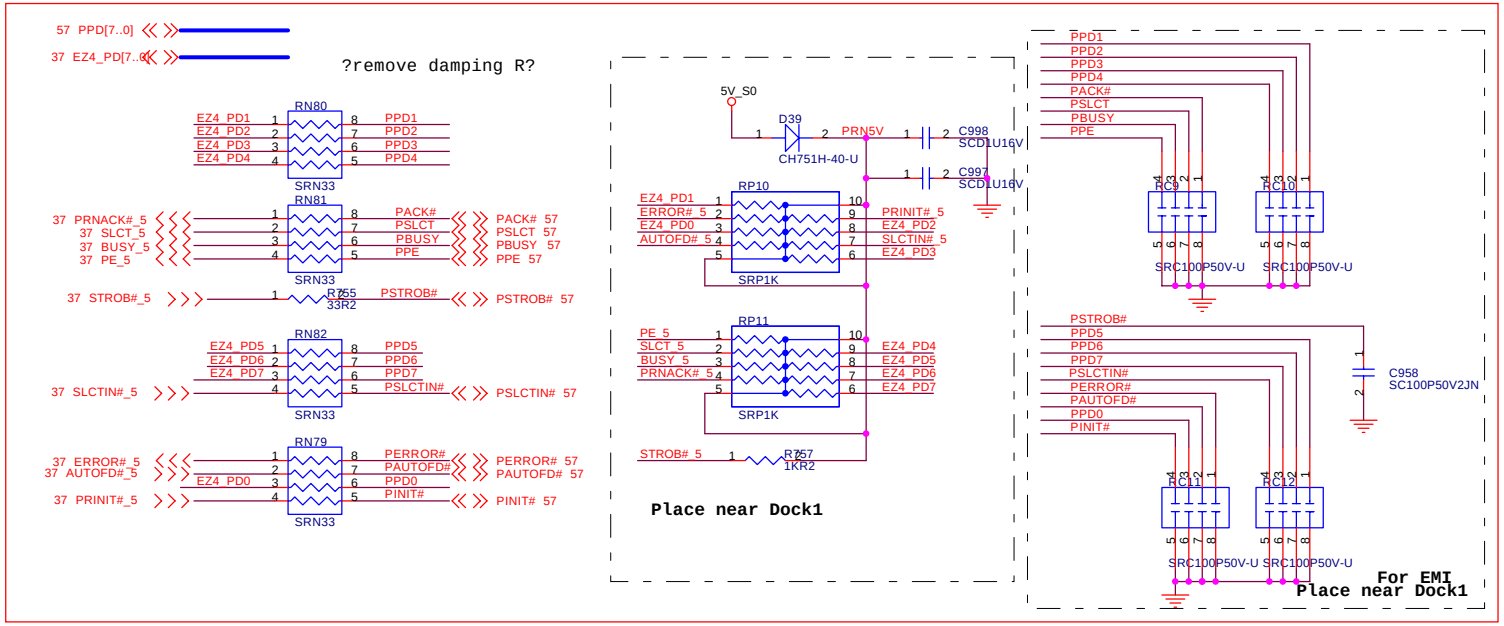
PRINT PORT



Dummy when no EZ4

華創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***EASY PORT4 (2/2)***

Size	Document Number	Rev
A3	Bolsena	SA

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